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SIMULATION GETS SPEED, CAPACITY BOOST

Page 26

STACKABLE ARCHITECTURES DIVERGE

Page 22

LITHIUM-ION BATTERY CHARGER PROVIDES USB OTG CAPABILITY

Page 34

MODERN ADCs IMPROVE CMOS IMAGE SENSORS

Page 38

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Green Engineering

MEASURE IT – FIX IT

La Selva Biological Station developed a wireless sensor system to monitor the rain forest ecosystem.

Nucor Steel optimized its steel melting process to drastically reduce electricity consumption.

CEMS Engineering built a control system to reduce energy use of industrial air chillers by 30 percent.

Vehicle Projects created a complex control system for a zero-emission, fuel-cell-powered locomotive.

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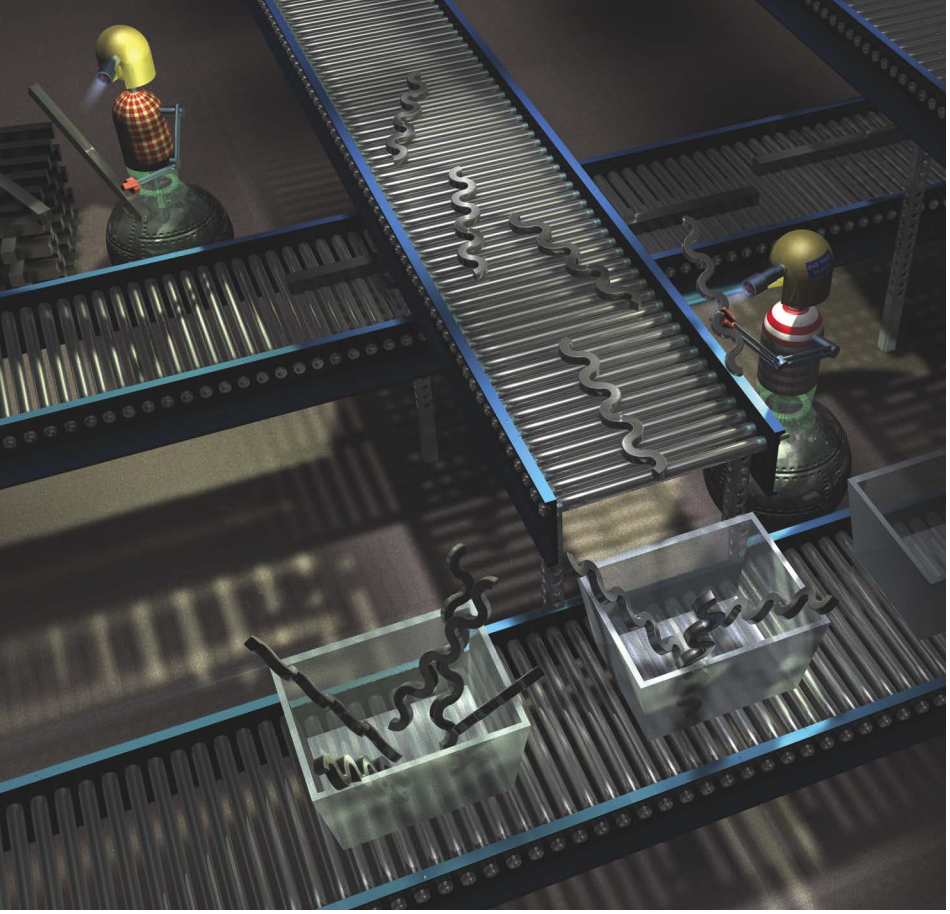

EDN contents

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Lithium-ion battery charger provides USB OTG capability

 With users demanding communication among their mobile devices, supporting the power needs of USB OTG (On-The-Go) becomes a requirement. Optimize your battery chargers for a current-limited source, such as USB, and for supporting USB OTG specifications.

by Jinrong Qian, PhD, Texas Instruments

Modern ADCs improve CMOS image sensors

 IC designers have improved the ADCs inside CMOS sensors, which must capture frames quickly enough for high-definition video. With this constraint in mind, designers must weigh the benefits of ADC architectures and make trade-offs in speed and size.

by Randy Torrance, Chipworks Inc

Simulation gets speed, capacity boost

 Analog- and RF-simulation tools offer choices of simulation speeds and support hierarchical design strategies.

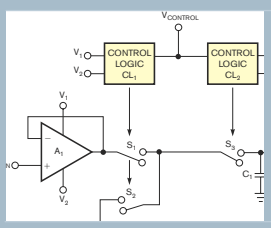
by Rick Nelson, Editor-in-Chief

Stackable architectures diverge

 Although standards organizations differ on updates to replace the obsolete ISA-bus technology, classic PC/104 continues to attract embedded-system designers.

by Warren Webb, Technical Editor

DESIGNIDEAS



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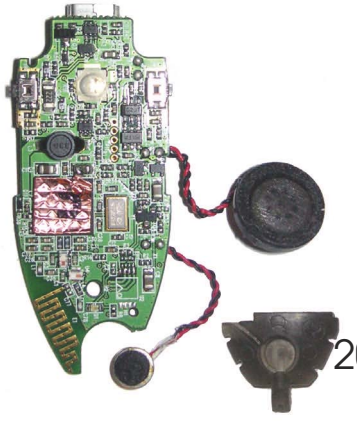
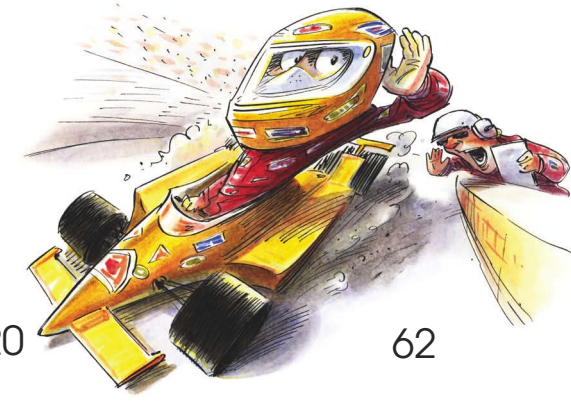
pulse

12



20



62

DEPARTMENTS & COLUMNS

PRODUCT ROUNDUP

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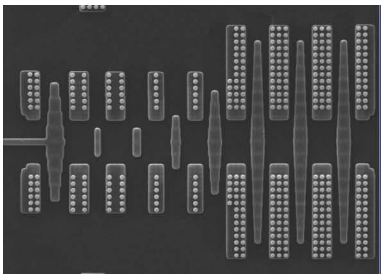

ONLINE ONLY

Check out these Web-exclusive articles:

Low-power wireless performance starts with CMOS elegance
The IC Insider delves into an ISM transceiver implemented in standard CMOS, revealing that interference-free operation in this crowded swath of spectrum begins with attention to layout details.
→www.edn.com/article/CA6626088

Evolving IP market spawns a raft of new approaches
Whether it's by asserting patent rights or defending against so-called trolls, entrepreneurs and investors are trying new IP business models.
→www.edn.com/article/CA6625809

EoPDH as an alternative for delivering rich-media applications
This study compares the performance of media-delivery techniques to show how EoPDH (Ethernet-over-plesiochronous-digital-hierchy) technology can deliver reliable, resilient transport services for streaming-video applications.
→www.edn.com/article/CA6624633

READERS' CHOICE

A selection of recent articles receiving high traffic on www.edn.com.

Life after layoffs: how to move forward after a job loss
Layoffs aren't fair, but they are a fact of life, or at least life as an engineer. With the number of job cuts continuing to rise and competition for open positions becoming more intense by the week, industry experts and career strategists share their advice on continuing an engineering career after being laid off.
→www.edn.com/article/CA6623840

The Hot 100 Electronic Products of 2008
→www.edn.com/article/CA6622869

Solar's bright future
→www.edn.com/article/CA6622867

Intel's Atom illness, and Nvidia's symptom-squelching adroitness
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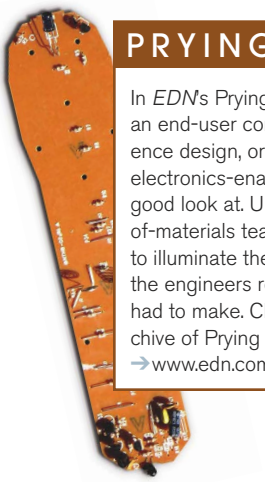
Prototyping techniques: things to know before pulling the trigger
→www.edn.com/article/CA6619017



PRYING EYES

In *EDN*'s Prying Eyes, we peer inside an end-user consumer gadget, a reference design, or any other interesting electronics-enabled thing we can get a good look at. Unlike your average bill-of-materials teardown, Prying Eyes aims to illuminate the tough design decisions the engineers responsible for the design had to make. Check out the entire archive of Prying Eyes.
→www.edn.com/pryingeyes

INNOVATION

VOTING OPENS FEBRUARY 2

Tune in to www.edn.com/innovation on February 2 to see the innovative engineers and products our editors selected as finalists in this year's *EDN* Innovation Awards. After perusing the candidates, help us honor electronic innovation by using the easy electronic ballot to make your voice heard.

BY RICK NELSON, EDITOR-IN-CHIEF

Evolution and innovation

What drives innovation, and can we harness the driving force to innovate our way out of our current economic difficulties? Next month, we at *EDN* will be asking you to help us identify the most innovative products and most innovative people of 2008. As I stated in June in our *EDN Innovators 2008* supplement, however, innovation is easy to recognize after the fact but difficult to schedule in advance.

In an effort to help create an environment conducive to innovation, we will continue this year to bring you profiles of innovators—in special supplements in March and June and in our "Voices" column in every other issue. Our hope is that you use some of their insights.

Meanwhile, Krisztina Holly, vice provost for innovation and executive director of the USC Stevens Institute for Innovation at the University of Southern California, has an interesting take on innovation in a Dec 16, 2008, Huffington Post blog item, "The Innovation Ecosystem." Had she been a venture capitalist at the end of the Mesozoic Era, she writes, she would have placed her investments with the adaptable mammals—not the dominant dinosaurs of the time, which were on an evolutionary path to extinction.

She then cites efforts to avert mass extinction of US auto companies. Should the government work to prevent this possible collapse or stand aside? Holly doesn't take a clear stand on this question. "Determining the right path is not easy, and either way the results will be painful," she writes. What interests her is how we can foster innovation to prevent the likely collapse of a key industry from recurring.

She believes that the rules of natural evolution are applicable to economically sustainable innovation. Holly writes, "Although I am the director of a leading university institute for innovation and a serial entrepreneur myself, in some ways I've learned as much about business life cycles by observing nature on my weekend mountain-bike rides. What I've seen is that a thriving ecosystem, whether in nature or economics, emerges from an evolutionary culture that nurtures diversity, doesn't artificially pick 'winners,' and embraces failure early and often."

Holly notes the irony ... that the decay of doomed Mesozoic life resulted in the formation of petroleum, "which ... fueled the internal combustion engine and today's failing auto industry."

She praises entrepreneurs, "the diverse and future-oriented thinkers that will advance our economy despite times of struggle. This group gives us the mutations—the radical changes that enable groundbreaking ideas to enter the ecosystem if they are worthy." But she adds that big companies have a role as well: "They help amplify—through acquisition, licensing, or even copying—the impacts of successful ideas."

The danger, Holly says, is in prematurely picking winners—before evolutionary mechanisms indicate the optimum approach. She further explains, "Death is inevitable in an ecosystem, and furthermore it can be healthy. It's this brutal process of failure that prunes out the weak from the herd." She quotes John Seely Brown, a visiting scholar at USC and the independent co-chairman of the Deloitte Center for Edge Innovation, as saying that failures "form the fertilizer for the next generation."

Holly notes the irony of the fact that the decay of doomed Mesozoic life resulted in the formation of petroleum, "which has in turn fueled the internal combustion engine and today's failing auto industry." She concludes, "I look forward to seeing what today's failures will fertilize." At *EDN*, we will be tracking innovation in the electronics industry for you throughout the coming year.EDN

Contact me at rnelson@reedbusiness.com.

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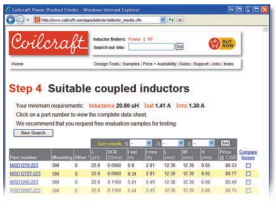

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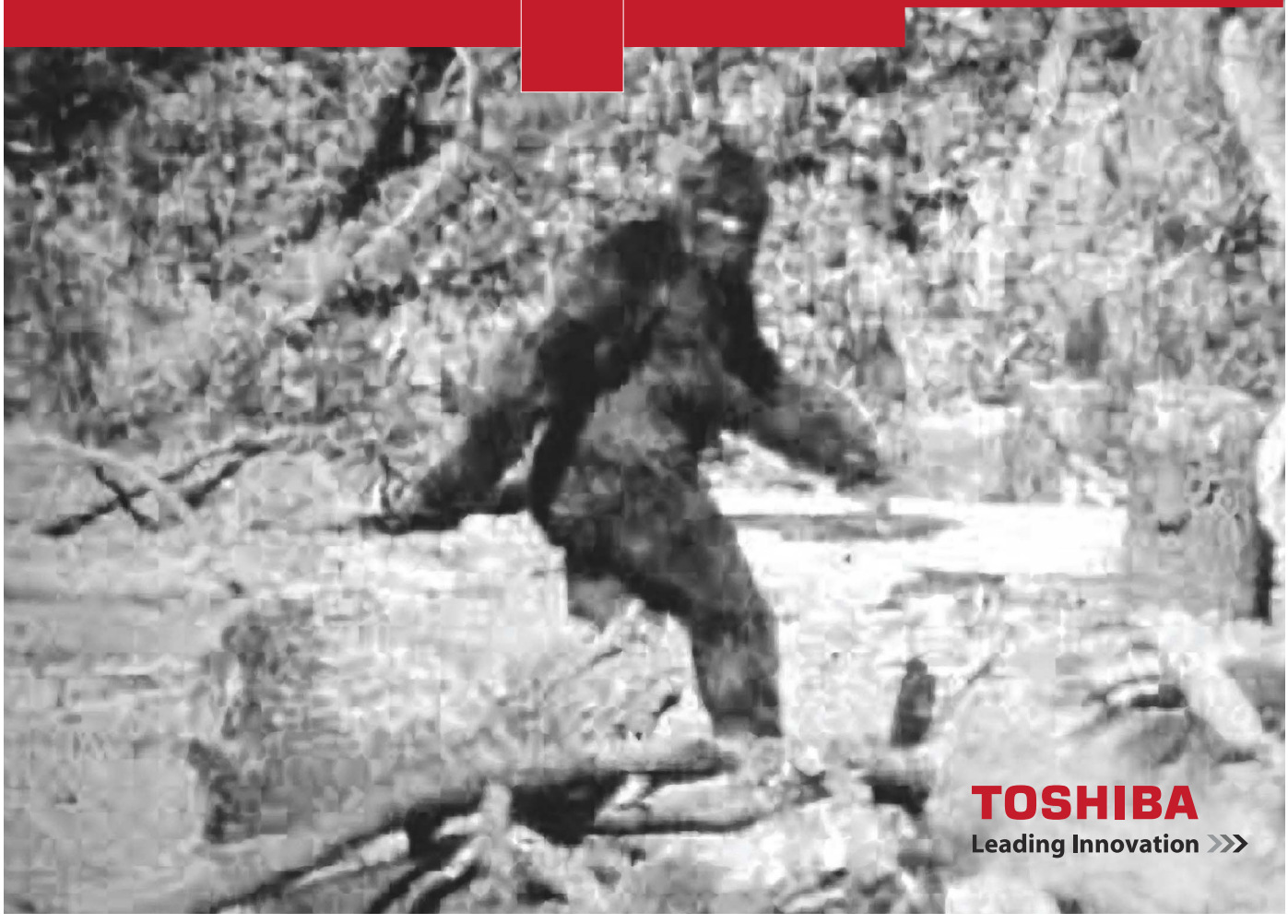

 photo credit: Roger Patterson

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pulse

INNOVATIONS & INNOVATORS

Flared-pin heat sinks use natural convection to cool "green" applications

Cool Innovations has introduced a line of flared-pin fin heat sinks featuring an array of sparsely configured round pins that slant outward, a configuration that cools components in natural convection environments. The rugged, forged-aluminum devices are suitable for harsh industrial and outdoor environments for applications such as solar cells and high-brightness LEDs. The flared-pin configuration offers a performance premium as great as 28% over traditional pin-fin heat sinks. For example, a flared-pin heat sink with a 1-in.^{2} footprint has a thermal resistance of 12.65°C/W, whereas a traditional heat sink with the same footprint has a thermal resistance of 16.14°C/W.

The omnidirectional spacing of the pins ensures that the heat sinks operate efficiently in any orientation. The heat sinks are available in square, rectangular, and round configurations, with footprints of 1×1 to 5×5 in. and heights of 0.7 to 2 in. Prices begin at $3 per unit.

—by Margery Conner

▷**Cool Innovations**, www.coolinnovations.com.

Flared-pin natural convection heat sinks can outperform traditional heat sinks by as much as 30% in applications relying on natural convection.

FEEDBACK LOOP

"If you want to be picky about what makes an SOC (system on chip): If it doesn't have all its operating code and if memory stores on the die, one might argue it is not a true SOC as microcontrollers are."

—Semiconductor engineer and *EDN* reader Ron Minemier, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6622874. Add your comments.

Technology squeezes the most power from solar-cell arrays

National Semiconductor plans to introduce the SolarMagic chip technology, which optimizes the power output from solar-cell arrays. The company expects the chip to be useful in the management of battery packs in applications such as EVs (electric vehicles) and HEVs (hybrid EVs).

Solar cells usually connect in series/parallel arrays. Solar radiation may not reach certain cells during certain parts of the day, reducing the available power from the series-connected string. The effect is greater than intuition would indicate: The company's figures indicate that approximately 10% shading—by area—can reduce power by as much as 50%.

The company employs its SolarMagic technology to disconnect the worst-performing cell in a series string and to deliver the maximum available power from the remainder. The technology then takes the reduced power available from that underperforming cell and adds it back—by dc/dc conversion—to the total power from the rest of the array.

In many scenarios, the company says, you can recover more than half of the power loss that the array would exhibit without this technology. The same strategy would be useful in extracting the maximum performance from EV-battery packs. In that situation, one battery cell that discharges more than the others in a series stack exhibits a lower voltage and higher internal resistance, reducing the output of the stack. You can use the same approach to extract all the available charge.**—by Graham Prophet**

▷**National Semiconductor**, www.national.com.

iPhone's popularity helps boost MEMS market

Apple Inc (www.apple.com) isn't the only company benefiting from the popularity of the iPhone. According to a recent report from iSuppli Corp, the handset is spurring competitors to offer products with comparable features, which in turn is fueling a sales boom for MEMS (microelectromechanical-system) accelerometers for motion detection in smartphones. "Apple's visionary use of MEMS accelerometers that support the automatic switch from landscape to portrait view on the iPhone display has prompted a flood of competitors to follow suit," says Jérémie Bouchaud, principal analyst for MEMS at iSuppli.

Handset makers are responding to consumers' demands for such devices. Early holiday-season data suggests that the Blackberry Storm (www.blackberry.com), a competitor to Apple's iPhone, would be among the most-purchased electronics for the gift-giving season. "Mobile-handset makers now are adopting accelerometers for this purpose and for other human-interface or power-savings applications, causing sales growth of MEMS for this application to exceed all expectations," says Bouchaud. "The mobile-handset industry has become the driver of the MEMS market, starting in the second half of 2008. This [occurrence] is truly a watershed event for the global MEMS business."

The research company estimates that, by the end of last year, 10% of the 1.29 billion mobile devices shipped worldwide would include MEMS accelerometers, up from 2% at the end of 2007. In total, the global MEMS-accelerometer market is expected to grow to 900 million units in 2012, up from 65 million in 2007. Global revenue from shipments of all types of MEMS for mobile handsets and smartphones will increase to $1.3 billion by the end of 2012, rising at a CAGR (compound-annual-growth rate) of 34.4% from $296.8 million in 2007, iSuppli further estimates. "Mobile-handset-accelerometer sales long have been driven by suppliers that are pushing the technology," Bouchaud says. "However, the market is now demanding this feature, preventing the MEMS industry from falling into the doldrums with most of the rest of the electronics market."

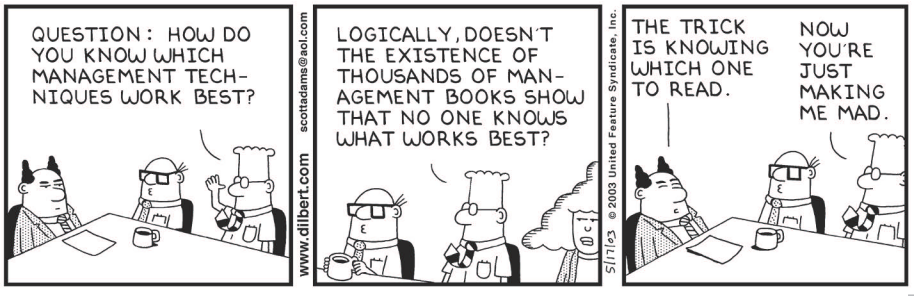
Accelerometer suppliers such as STMicroelectronics (www.st.com), Bosch (www.bosch.com), Analog Devices (www.analog.com), and Kionix (www.kionix.com) are the major beneficiaries of the increased use of MEMS accelerometers for mobile handsets. The market-research company also points to video-game-console controllers as other bright spots for MEMS gyroscopes and accelerometers, with their revenue growing at a CAGR of 11% to reach $240 million in 2012. The CAGR is thanks to their adoption in platforms such as the Nintendo (www.nintendo.com) Wii and Sony (www.sony.com) PlayStation 3.

> The mobile-handset industry has become the driver of the MEMS market, starting in the second half of 2008.

"MEMS motion sensors that detect free-fall in laptops to help protect their hard-disk drives have become standard features for commercial products and will begin to significantly penetrate consumer models in 2009," says Bouchaud. "Digital-MEMS microphones also will become more prevalent features in laptops to enhance VOIP (voice-over-Internet Protocol) applications. These two applications will grow at a CAGR of about 22% to reach $182 million in 2012, up from $68 million in 2007."**—by Suzanne Deffree**

▷**iSuppli**, www.isuppli.com.

DILBERT By Scott Adams



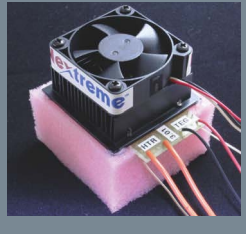
KIT EASES POWER-EVALUATION TASKS

The eTEG (embedded thermoelectric generator) power-generation-evaluation kit from Nextreme eases power-evaluation tasks in applications such as energy harvesting. The thin-film eTEG uses the Seebeck effect–the conversion of temperature differences directly into electricity in two metals in which a thermal difference produces a voltage across the two. The $295 evaluation kit provides a thick-film heater as a controllable heat source, the eTEG UPF40 power-generator module, a heat-sink/fan assembly, and thermocouples for temperature measurement. You need to provide only a power supply for the heater and a voltmeter to measure the voltage the eTEG generates across a load resistor.

The eTEG modules produce output power greater than 90 mW at a temperature differential of 70°C and greater than 260 mW at a 120°C difference. Measuring 1.6×3.2 mm, the eTEG module has corresponding output-power densities of approximately 5W/cm² at 120°C.

—by Margery Conner

▶**Nextreme, www.nextreme.com.**



The eTEG kit evaluates thermal-energy harvesting.

Scopes achieve 80G-sample/sec acquisition, bandwidth to 30 GHz

LeCroy's latest introduction, the 8 Zi line, includes WaveMaster digital oscilloscopes, serial-data analyzers, and disk-drive analyzers. The devices provide bandwidth as high as 30 GHz; acquisition of as many as 80G samples/sec; 512 million points of analysis memory, not including the acquisition memory; and edge triggering at more than 15 GHz. The devices also feature waveform analysis as fast as 100 times that of competitive units and a 15.3-in., 16-to-9-aspect-ratio, high-definition touchscreen display with 50% more area than that of 12.4-in. displays.

The units tout precise Eye Doctor signal-integrity tools and selectable 50Ω or 1-MΩ input impedance. The units also have TriggerScan rare-event-capture capability, removable front panels, optional integrated second displays, and external data-transfer rates as fast as 250 million points/sec—25 to 50 times as fast as other methods.

The 8 Zi line uses one hardware platform that the manufacturer configures as three series, which include 18 models with bandwidths ranging from 4 to 30 GHz. This approach lets you purchase only the bandwidth and features you need yet lets you keep pace with emerging high-speed technologies and serial-data standards by upgrading to greater bandwidth as your requirements change. This capability is attractive in today's lean economic times because it lets you pay initially for only the bandwidth you need but allows you to upgrade when necessary to 30 GHz of real-time bandwidth without paying for multiple instruments.

On units equipped for 20- to 30-GHz bandwidth, the standard acquisition rate is 80G samples/sec/channel on two channels when you use the full-bandwidth DBI (digital-bandwidth-interleave) mode. The patented DBI technology differs from time interleaving of ADCs and associated acquisition memory, which is common in high-performance real-time scopes. In addition, DBI provides wider bandwidth with lower noise, uncertainty, and waveform artifacts than do techniques that use digital-signal processing alone to extend bandwidth. The DBI-equipped scopes also let you use all four channels at reduced bandwidth. In that mode, the maximum acquisition rate is 40G samples/sec/channel.

> The SDA II tool set incorporates jitter-decomposition techniques and jitter-breakdown tools.

Within the WaveMaster 8 Zi series, scopes that lack DBI provide bandwidths of 4 to 16 GHz, with a maximum acquisition rate of 40G samples/sec on all four channels and an acquisition-memory depth of 10 million points/channel or, optionally, as much as 256 million points/channel. These scopes also offer the option of adding the DBI mode with its higher bandwidth and sampling rate. In the DBI mode, the acquisition-memory depth doubles to a maximum of 512 million points on each of the two channels.

For serial-data applications, the eight models in the 8 Zi SDA (serial-data analyzer) series offer the same 4- to 30-GHz bandwidth, sample rate, and analysis memory as the WaveMaster units but provide standard acquisition memory of 20 million points/channel. To test for compliance with PCIe (Peripheral Component Interconnect Express) 3.0 and USB (Universal Serial Bus) 3.0 standards, all SDA units also include a 3.125-Gbps serial-trigger capability, which operates on patterns as long as 80 bits, and the manufacturer's SDA II tools.

The SDA II tool set incorporates jitter-decomposition techniques and jitter-breakdown tools, which increase confidence in measurements and quickly provide detailed insights into device-under-test behavior. The SDA II tools also perform eye-diagram analyses as much as 100 times as fast as do competitive tools—capturing, analyzing, and displaying nearly 1 million unit intervals of PCIe activity in 3 sec. Additional tools, such as Iso-BER (bit error rate), which identifies constant-BER contours on eye diagrams, and the mask-violation locator, simplify understanding complex problems. To reduce timing and amplitude errors in high-speed eye diagrams, a cable de-embedding feature removes cable-induced distortion. The SDA 8 Zi units also provide complete, simultaneous views of eye diagrams, time-interval error, bathtub curves, jitter histograms, and other jitter-breakdown analyses. US list prices for 8 Zi scopes range from $59,490 to $209,490. Delivery for units without the DBI feature is eight weeks after receipt of order. For units with DBI, delivery is 26 weeks.

—by Dan Strassberg

▷**LeCroy Corp**, www.lecroy.com.

The 8 Zi real-time-sampling-scope line includes 18 models in three series. Of these, the fastest acquire 80G samples/sec/channel and faithfully reproduce 30-GHz-bandwidth signals.

Gallium-nitride technology targets power devices

International Rectifier plans this year to introduce a power-device technology employing gallium nitride on silicon. The company grows an epitaxial layer of gallium nitride on a conventional silicon wafer, and the gallium nitride forms the active devices in that layer.

Gallium nitride and silicon have significantly different coefficients of thermal expansion, as well as mismatched crystal lattices. One of the key problems that researchers have encountered in using silicon as an underlying substrate is getting the gallium-nitride layer to stay attached under operating stresses. International Rectifier has developed interposer layers that solve this problem. The company also asserts that, once it has overcome the adhesion obstacle, the economics of silicon—as opposed to other substrate materials that researchers have used, such as sapphire or silicon carbide—are compelling and open the way to volume manufacture of power transistors.

Unlike other experimenters in gallium nitride in the context of power devices, another thread of research deals with the material as the basis for RF-power transistors. International Rectifier begins with low-voltage transistors—for applications such as dc/dc converters—and progresses to higher voltages. "Other [companies and researchers] have worked with gallium nitride for high-power, traction-type applications," said Tim McDonald, vice president of emerging technologies, speaking at the Electronica 2008 trade fair (www.electronica.de) in November in Munich, Germany. However, the company believes that silicon carbide will likely take over that segment and that gallium nitride has a lot to offer for the high-volume, lower-voltage-product segment. The company intends this year to market products based on 30V transistors, following those products with 120V devices in 2010, and 600V parts in 2011.

> Gallium-nitride transistors have low stored charge and consequently low turn-off overshoot and transients.

Gallium-nitride technology offers substantially lower transistor on-resistance than the on-resistance that MOSFETs currently achieve. Today's FETs, McDonald says, are nearing some fundamental physical limits; with gallium nitride, a further reduction to approximately only 20% or even less of today's best values is feasible. Gallium-nitride transistors have low stored charge and consequently low turn-off overshoot and transients. With the reduced transients, EMI (electromagnetic interference) also diminishes proportionally. The basic device in the company's technology is an HEMT (high-electron-mobility transistor), a lateral device with conduction paths across the surface.

—by Graham Prophet

▷**International Rectifier**, www.irf.com.

EDN BLOG

POWERSOURCE

Chinese company begins selling HEVs

This month, BYD Auto began selling the first mass-produced plug-in HEV (hybrid electric vehicle). The plug-in hybrid version of its conventional F3 model, the F3DM (dual mode), went on sale in China for about 150,000 yuan (about $21,900). The company plans to bring the F3DM to the United States in 2010 and will show the car at this month's Detroit Auto Show. The F3DM has a range of about 60 miles on a full battery charge. Its lithium-ion iron phosphate batteries can be fully recharged in as little as seven hours, and the batteries can be 50% recharged at a special station in 10 minutes.

Warren Buffet, currently the holder of the undisputed title of the world's richest man since Bill Gates suffered some setbacks over the past month, rocked the Chinese financial markets on Sept 30, 2008, when a unit of Buffet's Berkshire Hathaway, MidAmerican Energy Holdings, invested $230 million in BYD Auto's parent company, BYD Co. BYD isn't making much public about its proprietary lithium-iron-phosphate battery technology that the company claims it developed for the F3DM, but most likely it gave more details to Buffet to get that kind of investment.

BYD said it may accelerate its plans for entering the United States and European markets by using MidAmerican Energy's money, with a larger version of the F3DM, the F6DM, available in the United States as early as 2010.

Here's what BYD Auto says about its battery technology on its Web site: "Top speed is over 150 km/hour; it takes less than 13.5 seconds to accelerate from 0 to 100 km/hour. The maximum gradability is more than 30%. The electric-power consumption is less than 12 kWhr per 100 km. The car can travel over 300 km per charge. Meanwhile, the battery's life cycle is about 2000 times/600,000 km for a complete vehicle." Note: These specs are for the "F3e," which is apparently an all-electric version of the F3DM. The range is listed at over twice that of the F3DM quoted in a recent *Wall Street Journal* article. According to AutoBlogGreen, Portland, OR, is romancing BYD to become the home base for US operations and possibly production.

—by Margery Conner

▶www.edn.com/powersource.

▶This is an updated version of an earlier post. For the original post, go to www.edn.com/090122ba.

ISSCC papers look toward high-definition handsets

An early look at papers to be presented at the 2009 ISSCC (International Solid State Circuits Conference) this February suggest the imminent arrival of HD (high-definition) video in your hand. Underlying technology in broadband communications to support the demanding data stream is now in silicon, and a new generation of HD-targeted media SOCs (systems on chips) is making its debut. Real HD in handsets—whatever the practicality of the medium in this format may turn out to be—cannot be far behind.

The foundation for HD video in a handset is sufficient wireless bandwidth to deliver the bit stream, coupled with sufficient band flexibility to work with whatever broadband signal is available at the moment. This requirement demands broadband transceivers—W-CDMA (wideband-code-division multiple access) and beyond—that are both effective and highly integrated. And at least three papers at the conference will speak directly to this need.

ST-NXP Wireless (www.stnwireless.com), the former and now merged wireless groups of ST, NXP, and Ericsson Mobile Platforms, will present a zero-IF receiver covering 3+4 WEDGE (wideband-CDMA-plus-enhanced-data-global-system-for-mobile-communication-environment) bands. The die operates without SAW (surface-acoustic-wave) filters on the front end, and you can integrate it into a 7×7-mm SIP (system-in-package) transceiver for production. The receiver consumes 92 mW.

Meanwhile, Skyworks Solutions (www.skyworks.com) and SpectraLinear (www.spectralinear.com) will present a 3G (third-generation) multiband-transceiver chip covering W-CDMA, HSDPA (high-speed-downlink-packet-access), HSUPA (high-speed-uplink-packet-access), and EGPRS (enhanced-general-packet-radio-service) standards. And Qualcomm (www.qualcomm.com) will introduce a single-chip UMTS (universal-mobile-telecommunications-system)/EGSM (extended-GSM) transceiver with integrated GPS reception, drawing only 69 mA. Both of these chips eliminate the need for SAW filters at key points, and both support receiver diversity.

> The focus has shifted from the latest process technology and the greatest speed to the lowest operating voltage and the most useful work per joule of energy.

As multiband transceivers shrink into single chips, application-level SOCs are preparing to handle the HD content at handset-compatible power levels. Taiwan's MediaTek (www.mediatek.com) will describe a Blu-ray-player SOC that the company designed from the algorithms up to be cost-effective in low-priced players. The 90-nm, smaller-than-8×8-mm die can perform an H.264 decoding, 60-frame/sec image generation, and HDMI (high-definition-multimedia-interface) 1.3 output to a display module with 1.6W power.

Whereas the MediaTek part appears to target handheld players, an application processor from Renesas (www.renesas.com) squarely targets handsets. The chip decodes H.264 into 1080p, 30-frame/sec video and consumes only 342 mW. The 65-nm die measures 6.4×6.5 mm.

Interestingly enough, none of these chips push the state of the market in process technology or clock frequency. As we prepare mobile devices for more and more challenging operating scenarios, the focus has shifted from the latest process technology and the greatest speed to the lowest operating voltage and the most useful work per joule of energy. Especially indicative of this trend is MediaTek's decision to examine its algorithms in light of the final cost-effectiveness of the SOC, rather than selecting an algorithm and then attempting to shoehorn the implementation into the final system requirements.**—by Ron Wilson**

▷**ISSCC**, www.isscc.org.

FEEDBACK LOOP

"Most engineers need to know not just what, but also *why*."

—Engineer and *EDN* reader Shane Kennedy, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6615600. Add your comments.

$39 USB TOOL EASES REAL-TIME DEVELOPMENT

A new Piccolo family of microcontrollers from Texas Instruments offers real-time-embedded-system designers a higher level of integration by combining the CPU and memory with a series of built-in peripheral modules, including a 12-bit ADC, ePWMs (enhanced pulse-width modulators), on-chip oscillators, analog comparators, communication interfaces, and general-purpose I/O.

To simplify development of Piccolo-based projects, TI recently announced the $39 controlStick evaluation tool in a USB-stick form factor. The device comes with a 32-kbyte limited Code Composer Studio IDE (integrated development environment) plus sample projects that walk through Piccolo microcontrollers' functions, from simply blinking an LED to configuring the ePWM peripherals. For more advanced applications, TI also offers a $79 experimenter's kit, which allows designers to develop and prototype complete Piccolo microcontroller-based projects.—by Warren Webb

▶**Texas Instruments, www.ti.com.**

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VOICES
Silicon Laboratories' Mark Thompson

Mark Thompson is the vice president for the microcontroller division of Silicon Laboratories, which manufactures high-performance, analog-intensive, mixed-signal ICs. The company's products include 8-bit microcontrollers, broadcast audio and video products, embedded modems, ProSLICs (subscriber-line-interface circuits), silicon direct-access arrangements, clocks, and oscillators. We recently asked him a few questions about supporting embedded developers. A portion of that interview follows. For an expanded version, go to www.edn.com/090122p.

You are one of a shrinking number of companies offering only 8-bit processor products. Your high-end, 8-bit offerings include heavy integration with high-performance analog peripherals. What do you see as the future for your 8-bit processing products, and do you see your product line expanding to include 16- or 32-bit processors?

A We're seeing good success with our current product offerings. We look forward to continuing to innovate and expanding into more market segments with the type of products that we have. We have a long list of projects that we could do or could work on. In general, we select projects based on return on investment.

Silicon Labs looks at markets less with regard to how many bits we have and more with regard to what problems our customers are having and how can we best solve those problems. Today, we have been pretty successful in solving our customers' problems using the 8-bit core that we have, which is a pipelined, high-performance core that is very cost-effective. The price of any given product varies widely based upon a large number of factors, including the peripherals on the chip, the pin count, the memory size, and any customized software that we need to write for our customers. We look at the things we can bring together to solve our customers' problems.

How much of a role is software taking in influencing your next choice in features to add to your system offerings?

A Software can definitely be a differentiating aspect of a product. We take the approach of building a flexible hardware platform and then exercising the flexibility in the hardware through the use of software. That [approach] enables us sometimes to more quickly solve a customer's problems. In general, we have built our systems and ensured that our tools are easy to develop with. I think this theme is a common one among many of

the companies in this business. Every company wants to have its products be easy to use and simple to design with so that customers have a quick and efficient experience. I believe we have achieved that goal. We have some very nice development tools, including USB-tool sticks that make it easy to explore products, figure out how they work, write software for them, and get your applications into production.

You can offer flexibility in several ways—number one, with the variety of peripherals that you offer and, number two, with the ranges that those peripherals can support. If you can build in fairly wide ranges with regard to many of the peripherals, whether they be analog blocks, temperature sensors, ADCs, or capacitive-touch sensors, … then, the customers are not necessarily limited to a strict range. If they want to vary the capacitance on a capacitive-touch-sensor application and your product is designed from the get-go to handle a wider range of options, then you can exercise those ranges through software and select something that matches the customers' needs.

We often find ourselves partnering with our customers in helping to write either drivers or application software running on the microcontroller itself. Our approach is: We want to partner with the customer and help solve the problem. Does the customer need application software, hardware support, or testing support? Whatever it is, we want to help that customer with that problem so that the customer can get into production as fast as possible.

Are you seeing processors becoming more generalized or specialized?

A We can solve customer problems in multiple ways, but several general trends that we continue to see are that customers want cost-effective, easy-to-use solutions in a time frame that meets their needs. In general, specialization is one way to delve deeper into a customer's problem, better understand the factors surrounding that problem, and understand what it connects to. If you can wrap up some of those things into an overall solution for the customer, that [approach] can help them get to market faster. In one sense, specialization is a trend that we see and pursue.

Is energy efficiency a growth opportunity for small processors?

A In general, energy efficiency and power savings are macro trends on a worldwide basis. With the population expanding and the cost of oil being quite volatile these days, energy prices are fluctuating dramatically, and, in general, everybody would agree that saving energy or lowering the amount of power that you need is a good thing. We have a new line of low-power microcontrollers, which can operate down to 0.9V and act as supervisors for multiple processors for those types of applications that need to conserve power.

—interview conducted and edited by Robert Cravotta

BY BONNIE BAKER

Match sensor to converter or converter to sensor

The initial design approach you might take for an analog-to-digital-converter system is to look at the resolution you need and use an ADC that gives you a comparable resolution. To achieve the required accuracy or precision, add the necessary gain modules to the system so that the analog range of interest covers the dynamic range of the ADC.

There is an alternative, however: You can use a 24-bit converter to eliminate gain modules as well as the contributed offset, drift, and noise that you find in a 12- to 16-bit system. The 24-bit converter leads to a simpler approach. Additionally, you can achieve better performance for about the same or lower cost.

You might finish the design by using only a portion of the 24-bit ADC range. That's right: You might throw away bits! And you will still achieve or improve the resolution and accuracy of the original 12- or 16-bit system. The 24-bit converter gives an immediate system-gain advantage of 4096 over a 12-bit ADC, as well as an additional PGA (programmable-gain-amplifier) function. The internal PGA function in the delta-sigma converter can increase the gain by another—product-specific—factor of 64 to 128.

As a first step in the design process, you often look at the sensor that you are going to use. You then look at the sensor's output range and match the sensor's output range to the ADC's input. In this process, you need an analog gain cell to make the sensor/ADC match-up work. Alternatively, you may try to blindly find an ADC that matches the output range of your sensor. Be cautious of both strategies. Try to worry more about the *system* noise contribution, where the actual system resolution and accuracy are the important specifications.

For instance, if you have a 5V range with an analog gain of 250V/V with a 12-bit system, the system LSB is $5V/250/2^{12}$, or 4.88 mV (**Figure 1a**).

Now, put the sensor signal into a 24-bit converter with no gain (**Figure 1b**). You can use this strategy because the LSB size of the 24-bit system is equivalent to having an analog gain of 4096. When employing this approach, subtract out the effects of any analog level shifting by using the differential inputs of the ADC. This step allows you to apply a voltage to your negative ADC input and to position your positive-ADC input with the output of your sensor. Although the total range of the 24-bit ADC is operational, your sensor output might cover only a portion of the ADC-output codes. By selecting that portion of the ADC range, you can focus on the area of the signal response. Having a 24-bit ADC with an effective resolution of 23 bits is like placing 2048 12-bit converters across the range of the converter.

Future columns will look at implementing these ideas in load-cell and temperature-sensor applications. In both cases, I will compare the systems' performance and cost. By evaluating a few types of low-speed circuits, I'll compare a 12-bit application and a 24-bit implementation and show the advantages of this new way of designing. EDN

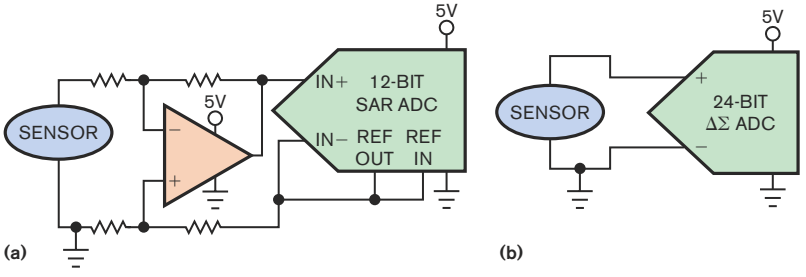

Figure 1 A 12-bit SAR converter (a) shows a sensor that connects through an amplifier to the converter. A 24-bit delta-sigma converter (b) shows a sensor that connects directly to the converter.

Bonnie Baker is a senior applications engineer at Texas Instruments and author of A Baker's Dozen: Real Analog Solutions for Digital Designers. *You can reach her at bonnie@ti.com.*

Go to www.edn.com/090122bb and click on Feedback Loop to post a comment on this column.

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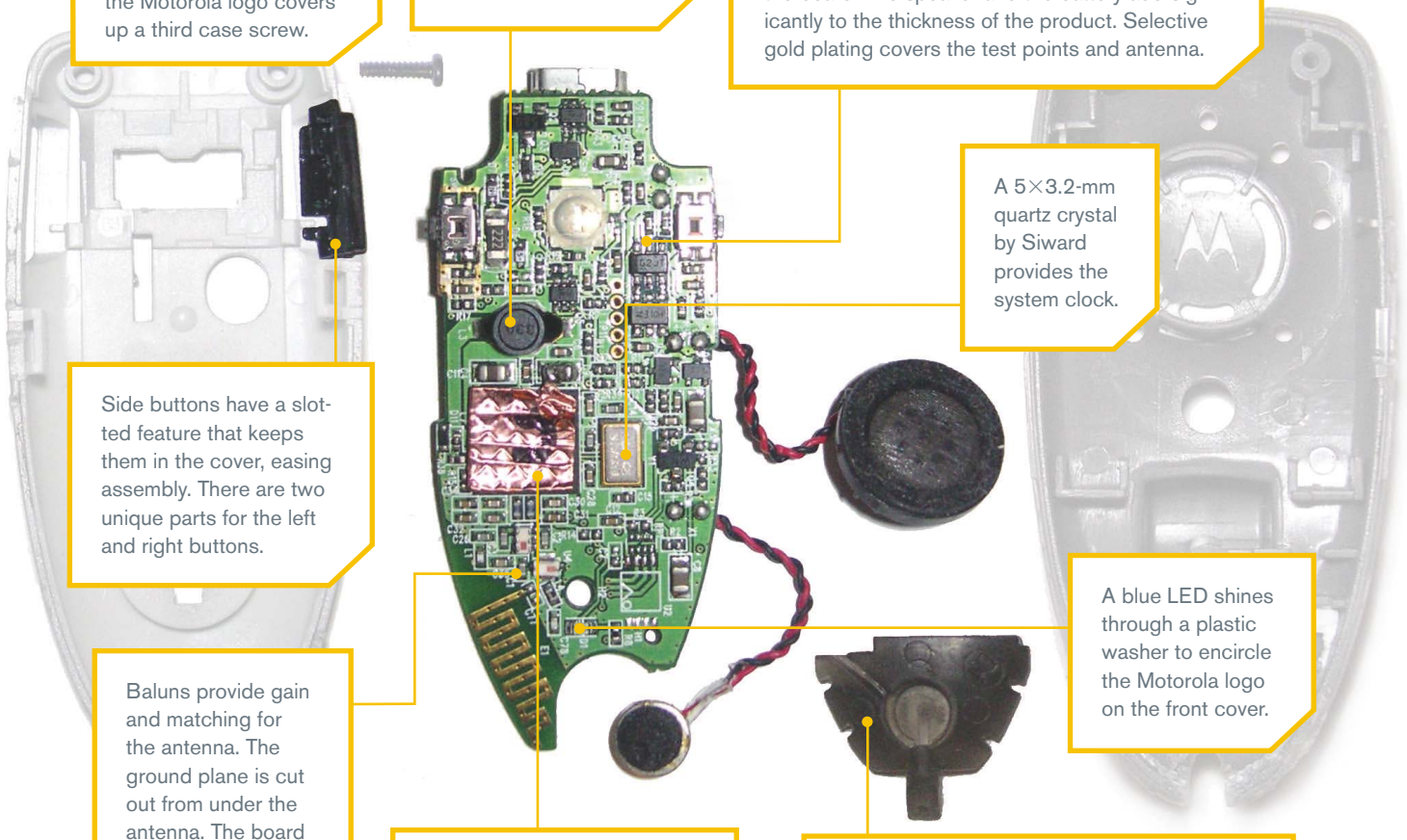
The Motorola H500 Bluetooth headset

While raking some leaves recently, I uncovered a fully charged Bluetooth headset. Someone's loss is someone else's gain, I thought as I pried into the interior of this popular consumer-electronics device.

Unlike some other Motorola Bluetooth headsets, this unit does not snap together. You pry off the black switch cover to get to two black screws; the Motorola logo covers up a third case screw.

The inductor's height required a hole in the front cover. This necessity may be due to the lack of 330-mH parts in low-profile packages.

All analog chips are in SOT-23-6 or SC70 packages. The backside of the board is nearly empty, which allows Motorola to glue the lithium-ion battery to it. There is no thermistor in the pack or on the board. The speaker and the battery add significantly to the thickness of the product. Selective gold plating covers the test points and antenna.



A 5×3.2-mm quartz crystal by Siward provides the system clock.

Side buttons have a slotted feature that keeps them in the cover, easing assembly. There are two unique parts for the left and right buttons.

Baluns provide gain and matching for the antenna. The ground plane is cut out from under the antenna. The board has a two-layer construction. The antenna is stitched to an identical trace on the bottom side.

A blue LED shines through a plastic washer to encircle the Motorola logo on the front cover.

The main chip is from CSR, a company that dominates the Bluetooth-IC business with nearly 80% market share. Copper foil is glued to the top of the chip and grounded to a decoupling capacitor.

A white-plastic microphone housing was glued to the back cover, necessitating its destruction. The housing captivates a rubber plug that holds the microphone. Extensive acoustic engineering accentuates your voice and attenuates bumps and ambient noise.

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ALTHOUGH STANDARDS ORGANIZATIONS DIFFER ON UPDATES TO REPLACE THE OBSOLETE ISA-BUS TECHNOLOGY, CLASSIC PC/104 CONTINUES TO ATTRACT EMBEDDED-SYSTEM DESIGNERS.

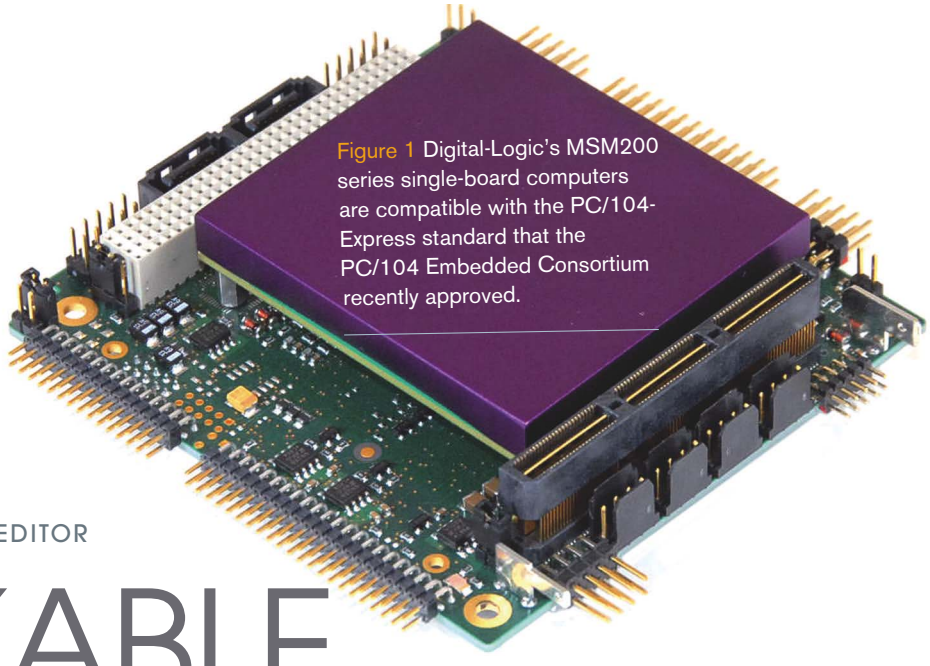

Figure 1 Digital-Logic's MSM200 series single-board computers are compatible with the PC/104-Express standard that the PC/104 Embedded Consortium recently approved.

BY WARREN WEBB • TECHNICAL EDITOR

STACKABLE ARCHITECTURES DIVERGE

With recent additions to the official specification plus multiple customized variations to extract more performance, PC/104-like architectures continue to be prime candidates for rugged and space-constrained embedded designs. These architectures could face troubled waters in the future, however. PC/104 has been a flexible and rugged favorite of the embedded-system industry since its introduction, allowing designers to choose from hundreds of off-the-shelf processor and expansion boards coupled with widely available desktop software to simplify system integration. Unfortunately, as users are increasingly demanding higher data rates for some applications, industry associations have not yet agreed on a strategy for the next generation of board-to-board communications. In addition, users content with the currently available data rates also face problems as the latest processor chip sets omit support for the legacy PC/104-bus architecture.

Ampro Computers in 1987 developed the original PC/104 concept to take advantage of low-cost desktop silicon and software for embedded systems. The company derived the name from the PC and the number of interface pins on the 16-bit ISA (industry-standard-architecture) bus. The company in 1992 published the first formal specification for PC/104, which the PC/104 Embedded Consortium currently maintains. PC/104 cards employ stack-through connectors that eliminate the need for a motherboard, a backplane, or a card cage. These pin- and socket-bus connectors provide a reliable signal path even in harsh environments. PC/104 cards have four corner mounting holes for board support to resist shock and vibration. Each card measures 3.6×3.8 in., and stacked-card spacing is 0.6 in.

Although the ISA bus has vanished from the desktop, it still has advantages for embedded systems. Many embedded-system designers are happy with prior-generation processors and the extinct ISA bus. Peripheral cards are simple, low-cost, and easy to design, all prime requirements of embedded products. The relatively low speed of the ISA bus also simplifies noise and EMI (electromagnetic-interference)-protection schemes. However, the main reason for its continued popularity is the fact that a large number of off-the-shelf products employ the architecture, giving designers a wide selection. Dozens of manufacturers now produce hundreds of unique, low-cost, off-the-shelf

PC/104 products (see **sidebar** "A new look at PC/104").

CHANGE THE BUS?

Since PC/104's introduction, designers have incorporated several enhancements to extend performance. The PCI (peripheral-component-interconnect) bus has effectively replaced ISA on the desktop, and it was only natural for system architects to add it to PC/104. The PCI bus brings a much higher data rate for high-performance peripherals and application-specific hardware. The PC/104 Embedded Consortium in 1997 released the specification for the PCI extension, formally known as PC/104-Plus. The specification gives board designers the choice of incorporating the ISA bus alone, the PCI and ISA buses together, or the PCI bus alone. PC/104-Plus requires a new connector, J3/P3, to house the PCI-bus pins. Because loss of board space is one of the disadvantages of the PCI upgrade, the PC/104 Embedded Consortium created the PCI-104 variation, which eliminates the ISA bus. The original PC/104 version continues to outsell both the PC/104-Plus and the PCI-104 updates.

To keep up with advances in technology and remain in tune with evolving desktop software, industry groups have put forth no fewer than three standards for the next generation of PC/104 development. These updates take advantage of the latest PCIe (PCI Express) specification, which the PCI SIG (special-interest group) defines, and USB (Universal Serial Bus) 2.0 technologies for higher data rates and improved board-to-board communications (see **sidebar** "PCI Express: the ideal fabric for stackable systems"). Although each of the new standards delivers substantial performance improvements in stackable architectures, the resulting products do not interoperate, and each provides varying degrees of compatibility with legacy PC/104 products.

The PC/104 Embedded Consortium agreed on the PCI/104-Express specification in early 2008 to define a standard method for using the high-speed PCIe

AT A GLANCE

- The size, rugged configuration, low power, low cost, and availability of PC/104 modules make them effective embedded-system-development platforms.
- Even though developers based the 20-year-old PC/104 architecture on the fading ISA (industry-standard-architecture) bus, it continues to outsell higher-speed extensions, including PC/104-Plus and PCI-104.
- Recent specification proposals for PC/104 updates have included PCIe (Peripheral Component Interconnect Express) or USB (Universal Serial Bus) communications to maintain compatibility with PCI-based software.
- New PC/104-form-factor updates sacrifice direct legacy compatibility to boost computing and communications performance and retain board real estate.

A NEW LOOK AT PC/104

By Christine Van de Graaf, Kontron

Design budgets address more than cost. When they consider development time, enclosure space, and performance factors, PC/104 or PC/104-compatible systems can be effective choices. Ideal for designs that require little–if any–hardware customization, PC/104 and PC/104-compatible systems are stable platforms that have evolved to deliver increased performance within small form factors.

A stable platform allows designers to interchange PC/104 products from vendors, perhaps to capture a performance jump they couldn't achieve with a product they implemented in years past. The fact that manufacturers keep components in the same place on a board is probably one of the most important advantages of working with an industry-standard product and one that makes it simple for designs to evolve from older PC/104 to newer PC/104 architectures. Further, some manufacturers keep features consistent from module to module, which avoids complicating the interior of the enclosure due to the added cabling that PC/104 designs require. PC/104 signals use pin-through rather than plug-in connectors; cabling then brings the signal through to the outside. Alternatively, the designer incorporates a carrier board with its own plug-in connectors.

A PC/104 stack typically has a maximum of six boards. So, a designer places the CPU board atop the baseboard with all the connectors. If the CPU board lacks a feature, a common issue in some vendors' boards, the designer must use another block of boards on top. The next block could include graphics, another could include sound, and another could employ Ethernet or Firewire. More advanced boards can reduce the size of the stack. Some have built-in I/O capabilities so designers don't need a separate PC/104 board with graphics, Ethernet, or sound, for example. Using more functional and properly selected boards can quickly reduce your stack from six small-form-factor single-board computers to just two.

PC/104 has other advantages in, for example, designs that require moderate performance with a small budget. And, if a design uses a PC/104 board, the designer's tendency would be to stay within the same technology area. Tight budgets and small enclosures could mean some trade-offs to stay with the same platform, but advances in PC/104 have improved the potential in this area. Not all PC/104 boards are created equal, and some are just more advanced than others.

AUTHOR'S BIOGRAPHY

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bus in embedded-system applications. The basic PCIe link consists of two signal paths that use LVDS (low-voltage-differential-signaling) swings and constant-current line drivers to communicate at a rate of 5G transfers/sec in each direction. You can increase the bandwidth of an individual PCIe link by adding signal pairs, or lanes, until you reach the desired performance level. Although the PCIe specification defines one-, two-, four-, eight-, 16-, and 32-lane widths, the PCI/104-Express specification supports only four one-lane links and one 16-lane link.

Digital-Logic offers several PCI/104-Express cards, including the MicroSpace MSM200 series single-board computers (**Figure 1**). The modules come with the Intel Atom processor operating as fast as 1.6 GHz plus several options for onboard RAM. The modules target applications in battery-powered mobile computers, information terminals with video displays, game systems with music output, measuring instruments, and telecommunication devices. Besides the fast CPU, the MSM200 provides all standard PC interfaces for such demanding applications, including Ethernet, an audio controller, four RS-232 interfaces, and two serial- and one parallel-disk interface. Prices for the MSM200 start at 364 euros (approximately $520) per unit (100).

EXPRESS104

Taking a different approach, a recently formed industry trade group, the SFF SIG (Small Form Factor special-interest group) in early 2008 defined the Express104 PC/104 extension. These boards incorporate one or two newly developed 52-pin SUMIT (stackable-unified-module-interconnect-technology) connectors. One of the connectors provides two one-lane links and one four-lane link, plus three USB 2.0 interfaces, a low-pin-count bus, dual SPI (serial-peripheral-interface) channels, an SMBus (system-management bus), and a set of ExpressCard interface signals. The optional second connector provides another set of one- and four-lane links. Express104 also supports an optional

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PCI EXPRESS: THE IDEAL FABRIC FOR STACKABLE SYSTEMS

By Steve Moore, PLX Technology

Many types of SFF (small-form-factor) embedded-system applications use stackable architectures to enable system and I/O expansion without the need for backplanes or card cages. The interconnect element for stackable systems has over the past 16 years migrated from ISA (industry-standard architecture) to PCI (peripheral-component interconnect). Now that the PCI/104-Express standard is available, embedded-system designers can take advantage of PCIe (PCI Express) technology to deliver lower cost and power consumption, smaller boards, less cabling, fewer connectors, higher data throughput, lower latency, and legacy-PCI-software compatibility that greatly simplify the transition to PCI/104-Express.

Thanks to broad silicon availability resulting from PCs, servers, and workstations adopting PCIe, the sheer volume of PCIe devices has surged, dramatically reducing their costs. The reduced power consumption comes from the fact that a 250-Mbyte/sec PCIe link uses only four wires–one transmitter pair and one receiver pair. Contrast this number with the cost and link requirements of the 32-bit PCI bus, which requires more than 100 I/Os and which delivers a maximum of 125 Mbytes/sec. This substantially lower I/O count also accounts for the reduced pin count on the PCIe chips, meaning reduced board space, smaller connectors, and improved PCIe cabling.

Designers are already using widely available PCIe Generation 1, which operates at 2.5G transfers/sec, and Generation 2, which operates at 5G transfers/sec, switches from vendors such as PLX Technology to build higher-performance interconnect fabrics within PCI/104-Express-based stackable/SFF systems. PCI/104-Express calls for four one-lane PCIe Generation 1 links, each capable of 250-Mbyte/sec transfers–twice the bandwidth of 32-bit, 33-MHz PCI that PCI/104 uses. You can also use Generation 2 switches because they automatically downlink to Generation 1. This speed gives stackable/SFF systems a significant I/O bandwidth boost, yielding a much faster fabric. Additionally, it provides as many as four high-speed I/O channels that need not share bandwidth across a single bus, as with PCI/104. PCI/104-Express also specifies a 16-lane PCIe link, providing a throughput boost of more than 32 times that of the PCI 32/33 standard.

Designers have applied other I/O interconnects, such as USB and GbE (gigabit Ethernet), but neither approaches the throughput capabilities and low latency of PCIe. A high-speed USB 2.0 connection, for example, can support only 40 Mbytes/sec, compared with the slowest, one-lane Generation 1 PCIe link, which delivers 250 Mbytes/sec. GbE supports only 125 Mbytes/sec with a high-latency overhead, whereas the fastest, 16-lane Generation 2 PCIe link provides throughput as fast as 10 Gbytes/sec.

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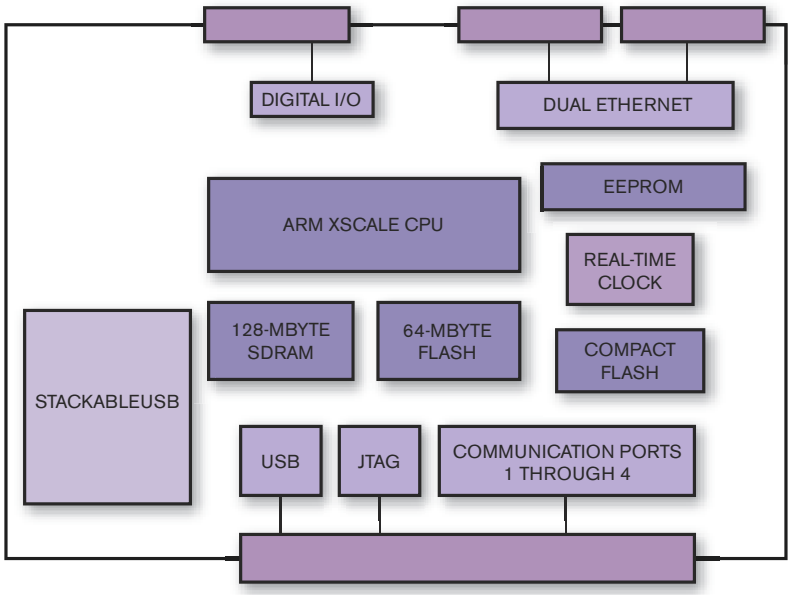

Figure 2 The SBC1626 single-board computer from Micro/sys combines a fast Intel XScale processor, memory, and StackableUSB I/O on a PC/104-form-factor board.

configuration that includes a PCI-to-ISA-bridge chip to retain compatibility with legacy PC/104 boards. Although several manufacturers have shown interest, none had publicly announced Express104 modules as of late 2008.

Offering yet another approach to enhancing the communications protocol, Micro/sys Embedded Systems created a new stackable architecture that it based on the PC/104 form factor. StackableUSB employs USB and retains the size and stacking advantages of PC/104. StackableUSB supports as many as 16 peripheral boards, takes advantage of USB plug-and-play features, and eliminates the need for a cable with a built-in stack-through connector. Micro/sys recently introduced the SBC1626 network-ready controller, which it based on the 104 form factor with seven USB ports, including five host ports through the StackableUSB connector and two client USB ports (**Figure 2**). In addition to its networking functions, the ARM-based SBC1626 also features 24 digital I/O lines, eight readable DIP switches, eight LEDs for application use, and four RS-232 ports; 64 Mbytes of onboard linear flash and 128 Mbytes SDRAM accommodate high-level operating systems, such as Linux or Windows CE. Prices for the basic SBC1626 start at $450 (one).

For standard performance, embedded-system designers will continue to specify and integrate classic PC/104 as long as legacy products are available. In addition, manufacturers will continue to produce these products as long as their board designers can find ways to link newer silicon to the obsolete ISA bus. For higher-performance applications, an update is necessary. Unless the industry chooses a successor to PC/104, the architecture will most likely enter a fragmentation phase, with manufacturers producing incompatible products. In the meantime, classic PC/104 lives on. EDN

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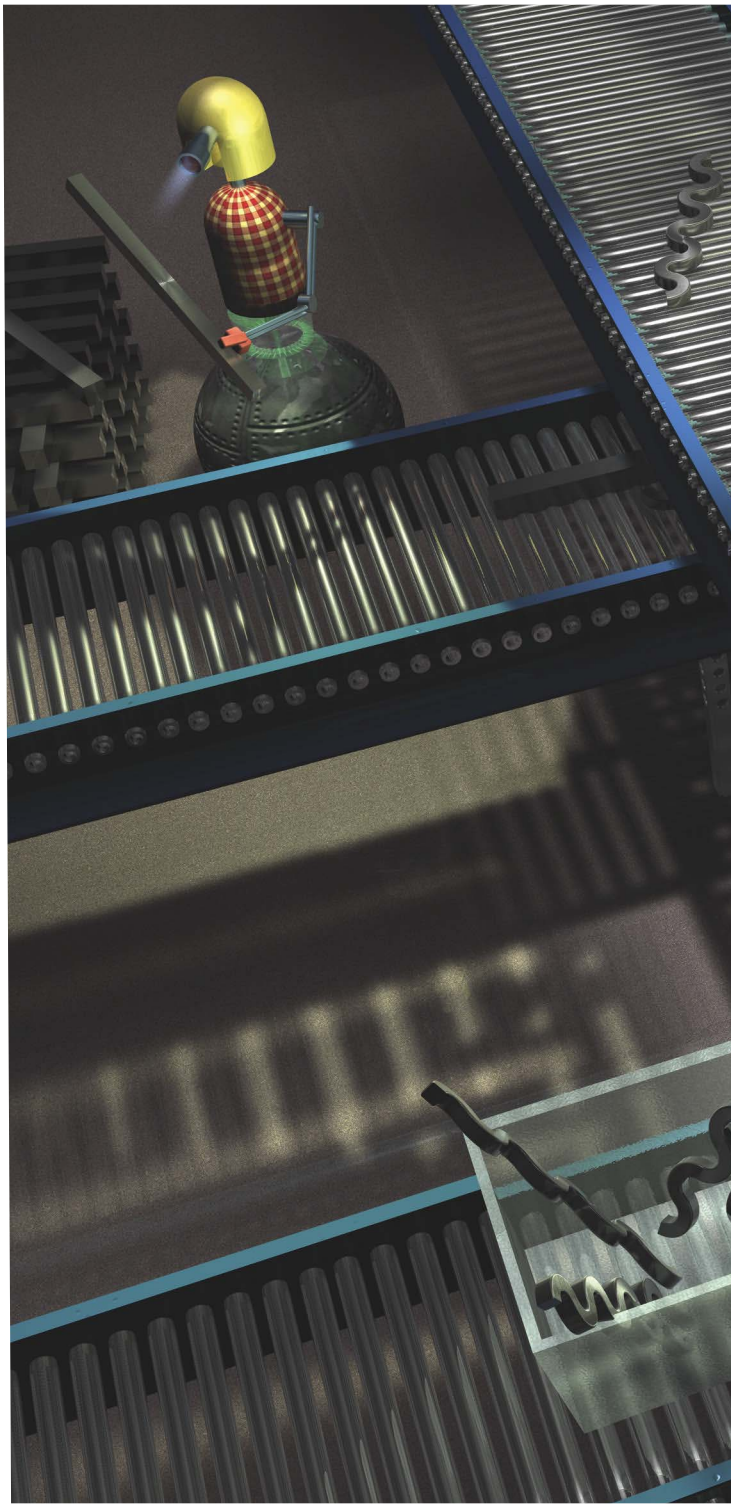
SIMULATION GETS SPEED, CAPACITY BOOST

BY RICK NELSON • EDITOR-IN-CHIEF

ANALOG- AND RF-SIMULATION TOOLS OFFER CHOICES OF SIMULATION SPEEDS AND SUPPORT HIERARCHICAL DESIGN STRATEGIES.



Speed, accuracy, and ease of use are key demands of designers employing simulation to get their analog-, RF-, and mixed-signal devices to market. Flavors of the venerable Spice simulator remain the tools of choice for analog simulation, and EDA vendors are enhancing the speed and accuracy of their tools through innovative techniques, such as adapting them to run on multicore processors or multi-CPU systems. Other companies are rewriting core Spice algorithms to speed simulations. Still others are focusing on top-down designs.

But Spice remains only part of the simulation picture as designers add RF/wireless-communications capability to an increasing array of products. And even products that offer no RF/wireless features are exhibiting RF performance as process geometries shrink, digital speeds increase, and high-speed serial-I/O ports proliferate. Furthermore, in many cases, as frequencies rise and designers squeeze more functions into smaller and smaller spaces, chip and board design cannot occur in isolation; co-design and simulation of chip, chip package, and board must take place.

How-Siang Yap, a member of the EDA-product-marketing group at Agilent Technologies' EEsof division, outlines the cross-domain-simulation technologies that can contribute to an effective co-simulation approach. First, he says, you need nu-

meric-domain tools, such as The MathWorks' Matlab or Agilent's Ptolomy, as well as C++, System-C, and standard HDLs (hardware-description languages). You also need frequency-domain ac-simulation tools that can work with S parameters and implement harmonic-balance techniques. For the time domain, Yap adds, you need Spice tools. Before committing your design to hardware, he advises, you should employ EM (electromagnetic)-domain tools that can apply method-of-moment and finite-element-analysis techniques to troubleshoot proximity and transition effects.

SPEEDING UP SPICE

As for Spice itself, efforts center on improving speed without compromising accuracy. Addressing this issue, Cadence Design Systems last month announced the availability of the Cadence Virtuoso APS (Accelerated Parallel Simulator), its next-generation circuit simulator, which constitutes a part of the Cadence MMSIM (multimode-simulation) 7.1 release. John Pierce, senior architect at Cadence, says that the new simulator reduces mixed-signal-simulation turnaround time from days or weeks to a few hours. According to Nebabie Kebebew, a senior product manager at Cadence, the new simulator provides significant single-thread and scalable-multithread performance boosts and maintains accuracy equivalent to that of the Cadence Virtuoso Spectre circuit simulator. Kebebew says that more than 20 beta customers have tested the new simulator on more than 200 designs for devices including PLLs (phase-locked loops), DACs, ADCs, memory, power-management circuits, and high-speed I/O circuits. One customer, she says, experienced a 60-fold performance speedup for the simulation of a 65-nm PLL design running on an eight-core system. Another, she adds, experienced 58-times-better performance for the postlayout simulation of a dc/dc converter, reduc-

AT A GLANCE

- Before committing your design to hardware, employ EM (electromagnetic)-domain tools that can apply method-of-moment and fine-element-analysis techniques to troubleshoot proximity and transition effects.
- Fast-Spice tools tend to trade accuracy for speed, but manufacturers often market these tools with a "Spice-accurate" label.
- Traditional Spice simulators run out of steam after a few hundred thousand elements, and even with parallel processing, capacity cannot improve.
- As manufacturers of consumer products strive to provide higher functional density at lower cost, they are squeezing together digital, analog, and RF functions into small volumes, creating a need for chip, package, and board co-design and simulation.

EM SIMULATION: FROM PCBs TO HELICOPTERS

As products become more complex and operate at higher frequencies, it's increasingly important to investigate signal- and power-integrity issues to simulate EMC (electromagnetic-compatibility) and EMI (electromagnetic-interference) effects. Tools that can help include CST's (Computer Simulation Technology's) PCB (printed-circuit-board) Studio, which supports 2- and 3-D simulations and can determine skin effect in the time and the frequency domains. It can import IBIS (I/O-buffer-information-specification) models and interfaces Spice-equivalent tools. With the CST Cable Studio, it supports co-simulation of PCBs and attached cables.

The company integrates PCB Studio and Cable Studio within Studio Suite 2009 EM-simulation software, which enhances design throughput by automating optimization and by applying the most appropriate solver technology to a given problem (Figure A). Studio Suite 2009 supports transient-EM and circuit co-simulation, and it offers a 64-bit front end plus MPI (message-passing-interface)-based parallelization to speed the simulations of large and complex structures. It includes a transient thermal solver to simulate heating processes and employs a bioheat equation for realistic modeling of physiological cooling effects.

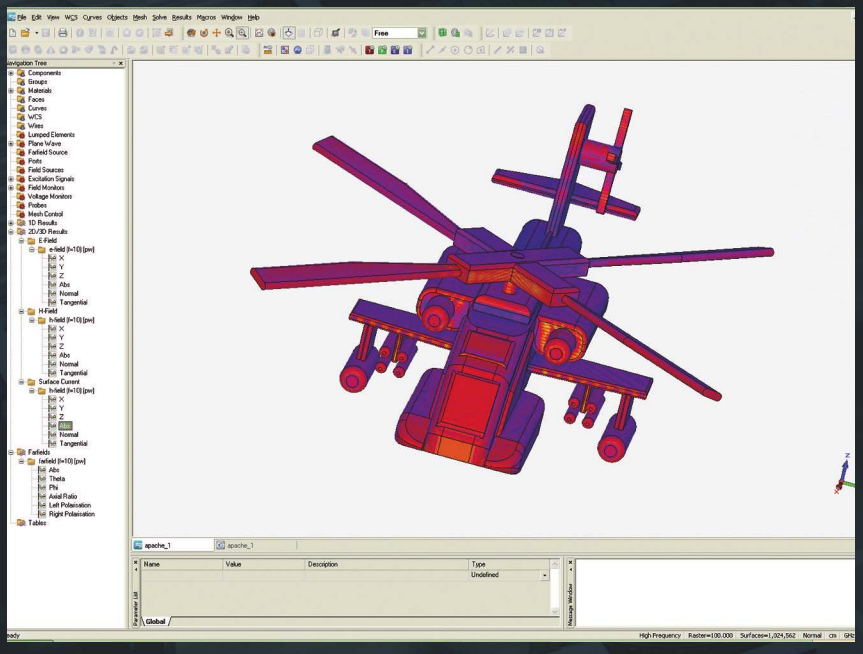


Figure A CST Studio Suite 2009 generated this simulation of the EM fields on the surface of an Apache helicopter to 10 GHz.

ing runtime from 20 hours and 16 minutes to 21 minutes.

Mentor Graphics has also been working to speed simulation. The company in October introduced a new version of the Eldo and Eldo RF transistor-level analog simulator, which improves raw-speed performance without compromising accuracy. The new version employs a revised matrix-solving strategy as well as a scalable multithreading technology that allows users to take advantage of inexpensive multi-CPU hardware.

According to Tony Liao, Mentor's deep-submicron-business-development manager, the multithreaded Eldo can run from three to 10 times or more faster than the single-core version, depending on the number of active devices and parasitic elements in a circuit. For faster simulation, he says, customers can employ the ADiT fast-Spice simulator, although at the cost of some accuracy. An ADiT-to-Eldo interface permits a circuit to run with both simulators; portions that require high accuracy run on Eldo, and the other portions run on ADiT. Liao notes that the simulators support co-verification through their links to Mentor's ModelSim digital simulator. The simulators' links to Mentor's ICAnalyst help support design verification. In addition, the simulators work together within Mentor's ADMS (Advance mixed-signal) simulator environment (**Figure 1**).

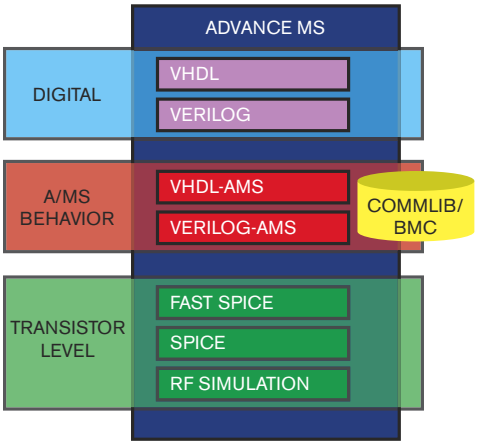


Figure 1 The ADMS (Advance mixed-signal) simulator from Mentor Graphics supports multiple modeling languages. The CommLib/BMC (behavioral-model-calibration) library contains parameterized analog- and mixed-signal models for communications applications.

Synopsys, too, has worked on speeding Spice and has announced improvements to its HSpice core-engine technology as well as new multithreading capabilities in the March 2008 release of its HSpice simulator. According to Geoffrey Ying, director of marketing for mixed-signal-simulation products at Synopsys, the company is adapting all its tools to take advantage of multicore processors, with HSpice being the first to migrate. He says that, with the multithreaded version, circuit designers can now run HSpice postlayout simulations as much as three times faster on single-core processors and as much as six times faster on four-core processors. The single-core speedup stems from improvements in the symbolic-dc-operating-point-convergence algorithm, transient time-step control, netlist parsing, and model performance. For multicore processors, the release enables simulation of postlayout designs containing more than a million resistive and capacitive parasitic effects.

Synopsys has worked with TSMC (Taiwan Semiconductor Manufacturing Co) on the TMI (TSMC Modeling Interface) methodology, which consists of a protocol for integrating custom device models into Synopsys' HSpice, HSim, and NanoSim circuit simulators. The TMI methodology delivers an innovative and efficient device-modeling approach for TSMC's process technologies at 40-nm and smaller geometries. Ying says that the TMI method, on average, improves simulation time and reduces memory usage by a factor of five and takes into account both mechanical-stress effects in silicon and layout dependencies that alter the characteristics of device instances based on their proximity to other devices.

Magma Design Automation uses multiple CPUs instead of multiple cores and multithreading. The company's FineSim Spice leverages Magma's NPT (native parallel technology) to enhance speed and capacity and maintain accuracy by distributing computing load over multiple computers, according to KT Moore, Magma's senior director of business development for the custom-design-business unit. The approach "enables customers to simulate hundreds of thousands of devices on practical numbers of computers—eight, not 100," he says.

Despite the performance increases of multithreaded and multicomputer implementations of Spice, a need for fast-Spice implementations will continue. "In different phases of a design process, the requirement for accuracy changes," Moore says. "Early on, you are more focused on functionality. As you narrow down your design to focus on the actual operating points and characteristics, then you want to tighten up the accuracy. A lot of large designs have millions of transistors; you could simulate [those transistors] using our Spice engine running on multiple CPUs, and that [approach] might be great for a sign-off simulation." He claims, however, that for regression or functional simulation, NPT is the tool you would probably want to use.

Traditional EDA companies are getting competition in the Spice arena from relative newcomers that at times blur the line between true Spice and fast Spice. For example, fast-Spice tools tend to trade accuracy for speed, says Paul Estrada, chief operating officer at Berkeley Design Automation. However, manufacturers often market these fast-Spice tools with a "Spice-accurate" label. Berkeley Design Automation's Analog Fast Spice, he claims, truly does provide fast-Spice capacity and performance with true Spice accuracy. The tool does no approximations, Estrada says. In-

TABLE 1 RELATIVE PLL SIMULATION TIMES WITH SPICE AND VERILOG-A MODELS

Phase detector	Charge pump	VCO	Divide by N	Relative CPU time
Spice	Spice	Spice	Spice	100x
Verilog-A	Spice	Spice	Verilog-A	64x
Verilog-A	Spice	Verilog-A	Verilog-A	13x
Verilog-A	Verilog-A	Verilog-A	Verilog-A	1x

stead, it runs original device equations and solves the original full-circuit matrix, providing waveforms that are as good as or better than those of any other Spice engine.

Analog Fast Spice provides its performance improvements running on a single-core processor. Estrada attributes its performance levels to the fact that its developers need not attempt to optimize legacy code. "Look under the hood at any of today's Spice engines," he says, "and you'll see that they are basically structured like a rat's nest. Everything is interwoven with everything else, and, if you try to improve one area of the simulator, you invariably make another area worse." Analog Fast Spice employs a modular architecture in which you can optimize each module without disturbing other modules. Looking to the future, the company is seeing good results with multithreading but hasn't yet released a multithreaded version.

Gemini is also employing multithreading to improve performance. The company targets 95% of the Spice-accurate-tool and fast-MOS-Spice market, says Kent Jaeger, vice president of sales and marketing. The Gemini holistic multithreaded Spice, he says, provides two- to 10-times better performance without compromising accuracy. "We forbade [our designers] to use any technique that would potentially sacrifice Spice accuracy." The Gemini simulator outperforms fast-MOS-Spice simulators in 90% of benchmark tests and runs on low-cost Intel multicore processors running the 64-bit Linux operating system.

Infinisim borrows some techniques from fast-Spice yet preserves Spice accuracy, according to the company's chief technology officer, Zakir Syed. The company's RASer (real-time-adaptive-simulation) simulator works at all stages of design verification—from single-block to full-chip and from prelayout to postlayout. According to Anand Iyer, senior director of marketing, RASer targets the critical need for doing total system simulation to avoid the need for silicon respins. "Traditional Spice simulators run out of steam after a few hundred thousand elements, and even with parallel processing, capacity cannot improve," he says.

Fast-Spice-like approaches come in handy at this point. "We break up [a circuit], just as fast Spice would, into smaller partitions, and then we apply different solvers to different partitions," says Syed. "In fast Spice, you lose accuracy, but … we use the exact device models that Spice uses."

Although Infinisim supports multithreading, the company focuses on speeding up individual threads. "Companies are developing multicore algorithms on Spice," Syed says, "and … these companies have given up on improving Spice." He says that, in some cases, such as Monte Carlo simulation, multithreading and distributed computing apply. In those cases, any simulation is independent of the other simulations.

"In analog designs, [we see] iterations in which you typically run five corner models and temperature sweeps," says Nicolas Williams, director of product management at Tanner EDA. "If you want to do Monte Carlo analysis, you [must] run thousands of simulations on your one circuit. It's easy to farm out those simulation runs from a single command deck." It's the simulation job level, not the circuit level, in which parallelization can offer the most benefits, he adds.

Tanner's T-Spice simulator aims at the design of big-analog, small-digital chips. The company has integrated Verilog-A to support both simulations with behavioral models and device-level Spice models. Verilog-A supports top-down design and offers significant advantages over the bottom-up approach that analog designers traditionally employ. Williams says that top-down design can eliminate costly and time-consuming design iterations that can be necessary when a bottom-up approach results in system-integration problems that occur late in the design cycle.

He notes that analog designers em-

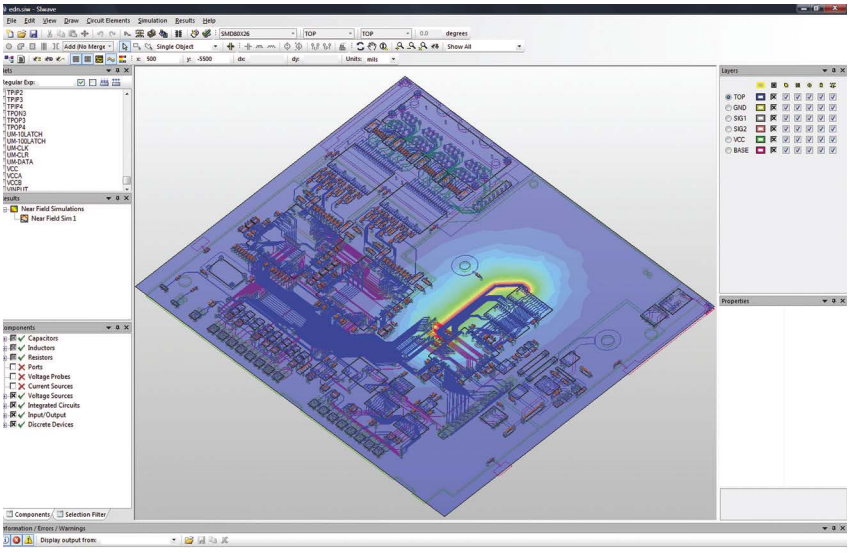


Figure 2 The SIwave tool can help identify and solve signal-integrity issues on PCBs (courtesy Ansoft).

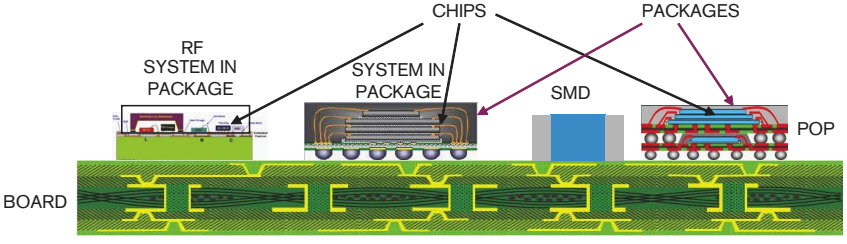


Figure 3 The efforts of consumer-product manufacturers to provide higher functional density at lower cost are resulting in the squeezing together of digital, analog, and RF functions into small volumes. That squeezing results in the need for chip, package, and board co-design using tools such as the Agilent EEsof ADS.

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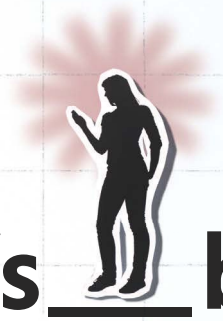

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ploy behavioral-modeling techniques when, for example, they use dependent sources, and they may use The MathWorks' Matlab to calculate coefficients, but, until now, they have lacked a behavioral language within a Spice-programming environment. The combination of Spice and behavioral models allows designers to focus on block design and perform simulations without lengthy runtimes. **Table 1** shows the relative CPU times for simulating a PLL with its components represented in various combinations of Spice and Verilog-A models.

BEYOND SPICE

Even a thoroughly simulated and verified chip design has no guarantee that a device will work properly when real silicon meets the real world. Silicon performance succumbs to the EM effects of the chip package, the board the package is mounted on, or the large-scale structure containing the board (see **sidebar** "EM simulation: from PCBs to helicopters"). Larry Williams, director of business development at Ansoft, recounts the story of a semiconductor manufacturer whose device worked on an evaluation board with nicely separated traces and lots of power and ground planes to isolate signals. However, the device exhibited abnormal behavior when the manufacturer's customer crammed it into a tiny consumer product in which the traces were much closer together, causing more coupling. All of a sudden, the chip's radio began to misbehave, generating unacceptable out-of-band spurious responses. "We worked to show how to solve the problem by using a complete system-level simulation of the chip, the chip package, and board," says Williams. Ansoft used the manufacturer's Spice-level model for the IC and performed 3-D extractions to create models of the IC's BGA package and the PCB (printed-circuit board). "We coupled all three together in our environment, and, lo and behold, we could predict those spurs," he says.

Ansoft's offerings include HFSS (high-frequency simulator system), which performs 3-D electromagnetic-field simulation of high-frequency and high-speed components, and SIwave (signal-integrity wave), which allows engineers to extract frequency-dependent circuit models of power-distribution and signal nets directly from device layout—that is, physical CAD (computer-aided-design)—databases to help identify signal-integrity and power-distribution problems (**Figure 2**). "The problems we solve are showstoppers," Williams says, adding that addressing SI is critical: "Companies are setting up SI departments to ensure reliable electronic performance. Look at any modern handheld electronic device; it may have several radios with a lot of digital content to provide a rich user experience. It will operate at low voltage to conserve power, and digital signals will consequently be sensitive to coupling. We allow an engineering design team to read in a PCB model, couple that with IC-package-model extractions, and cascade all

those things together to perform an entire system-level simulation."

EEsof's tools, including the ADS (Advanced Design System), had their origin with a group at Hewlett-Packard that developed RF and microwave instruments. ADS 1.0, which debuted in 2000, enabled designers to simulate RF circuitry along with digital circuits, including DSPs. The tool originally found extensive use in WLAN (wireless-local-area-network) designs and has continued to evolve. As manufacturers of consumer products strive to provide higher functional density at lower cost, they are squeezing together digital, analog, and RF functions into small volumes, creating a need for chip, package, and board co-design and simulation using ADS. EEsof's Yap cites two aspects of the co-design process: front end, which involves optimizing system partitioning for performance and cost, and back end, which deals with factors such as ball-pattern planning and routing plus I/O optimization.

A recent advance, he says, is support for nonlinear X parameters. Last month, Agilent announced that designers can generate X parameters either from simulation with ADS or from Agilent's test-and-measurement instruments to speed communications-product development. X parameters, says Yap, save significant amounts of time. With X parameters, a designer can acquire a model to use within a simulation. The alternative involves months of characterization and generates reams of plots that can be difficult to interpret.

As for the future, Yap sees continuing efforts to integrate electromagnetic simulation into the design flow to simulate everything from circuits to antennas. More products are going wireless, and, in compact products, the antenna is often on the PCB. The ability to identify potential problems before committing to hardware is critical, he says. **EDN**

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Lithium-ion battery charger provides USB OTG capability

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The USB (Universal Serial Bus) has been one of the most successful interfaces in the history of PCs. A USB not only transfers data between a portable device and a host PC, it also allows for power transmission over the USB cable. As a result, portable devices can charge lithium-ion batteries while connected to host PCs through a USB cable. You can power most of today's portable products from an ac adapter, a USB port, or a lithium-ion battery.

The USB 2.0 specification defines three modes of operation that allow peripherals to draw current from a USB. The suspend mode allows the peripheral to draw as much as 500 μA. The low-power mode defines the current consumption as high as 100 mA, and the high-power mode limits the current to 500 mA.

Traditional approaches use a low-cost linear-mode charger for USB charging. You usually disable the charger to meet the low-quiescent-current requirements of the suspend mode. The charger also has a current-selection function to set a charge current of either 100 or 500 mA. The charge current is equal to the input current from the USB output for a linear charger. So, the charge current is limited to 100 or 500 mA to meet the USB low- or high-power-mode specification. However, the charge-current regulation tolerance for most low-cost linear chargers is usually approximately ±10%. As a result, the actual typical charge current is set at approximately 90 or 450 mA to prevent it from exceeding the limit of the USB specification. This limit further curtails the charge current available to charge a battery from a USB port.

Most portable devices, such as smartphones, feature e-mail, personal organizers, touchscreens, built-in cameras, and navigation hardware and software. One common requirement is that they all demand more power for performing these advanced functions. Furthermore, the capacity of the lithium-ion batteries used in portable devices is consistently increasing, implying that USB charging time becomes longer due to the charge-current limit for a linear-mode battery charger.

A synchronous-switching converter efficiently uses the available power from the USB to charge a lithium-ion battery, shortens the charging time, and minimizes power dissipation to improve the thermal factors. This device has higher power-conversion efficiency and higher output-charge current for a given input current than does a linear-regulator charger. It steps down the voltage but provides a higher output current than input current.

Considering the power balance between the input and the output, the following **equation** yields the effective battery-charge current for a switching charger: $I_{CHG}=(V_{IN}/V_{BAT})\times I_{IN}\times\eta$, where I_{CHG}, V_{IN}, V_{BAT}, I_{IN}, and η are the battery-charge current, input voltage, battery voltage, input current, and power-conversion efficiency, respectively. This **equation** shows that a synchronous-switching converter provides a higher charge current at a lower battery voltage and a lower charging current at a higher battery voltage but always higher

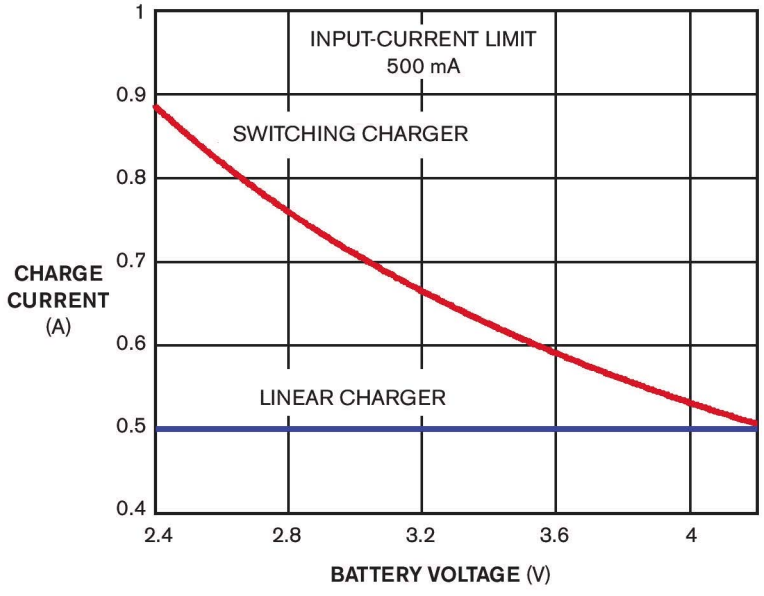

Figure 1 The switching charger can provide 40% higher average charging current than a linear-mode charger.

than the input-current limit when the input voltage is higher than the battery voltage. For USB charging applications, the input voltage is constant at 5V, and the input current is limited to either 100 or 500 mA. Thus, the charge current is inversely proportional to the battery voltage and proportional to power-conversion efficiency. A practical step-down, synchronous-switching buck converter can achieve about 90% efficiency.

Figure 1 shows the battery-charge current for a switch-mode, step-down charger and a linear-mode charger with a 5V USB input and 500-mA input-current limit. The switching charger can provide 40% higher average charging current than a linear-mode charger. **Figure 2** shows one example of a 3-MHz synchronous-switching, step-down charger, which integrates N-channel MOSFETs Q_2 and Q_3 that switch on and off at a 3-MHz switching frequency. Operating at this speed means that the circuit can use significantly smaller passive components—the output inductor and the capacitor. Thus, you can use the chip in size-constrained portable devices. N-channel MOSFET Q_1 blocks any leakage current from the battery to the input when the adapter is unconnected. You use a charge-pump circuit comprising bootstrap capacitor C_4 with an integrated diode to drive N-channel MOSFETs Q_1 and Q_2 and to charge capacitor C_4 when MOSFET Q_3 conducts. The integrated Type III loop compensator for battery-charge voltage and current loop further minimizes the need for external components and improves reliability.

You use the typical constant-current/constant-voltage-charging profile to charge a lithium-ion battery. A constant current of less than 1C charge rate—the current to completely discharge the battery in one hour—charges the battery when the battery voltage is below 4.2V for a battery with a lithium-cobalt-dioxide cathode and graphite-anode materials. It operates in constant-voltage mode to improve safety when the battery voltage reaches 4.2V while tapping down the charge current. The charge current and voltage are programmable through the I^2C (inter-integrated-circuit) communication protocol.

INPUT-CURRENT-LIMIT-REGULATION ACCURACY PLAYS AN IMPORTANT ROLE IN MAXIMIZING THE POWER AVAILABLE FROM THE USB PORT.

USB applications have limited input current. When the input current reaches the maximum current limit programmed by the I^2C, the input-current-regulation loop becomes active and reduces the PWM (pulse-width-modulated) controller's duty-cycle output by sensing current through MOSFET Q_1 so that it will comply with USB specifications. Input-current-limit-regulation accuracy also plays an important role in maximizing the power available from the USB port. With this method, you can achieve less than a 5% tolerance of MOSFET current sensing. **Figure 3** shows the experimental results for charging a lithium-ion battery through a linear charger and a switch-mode charger through a USB port. The switch-mode charger can shorten the battery-charging time by more than 10%.

SAFETY CONCERNS

Safety is a critical factor for consumer products. Input-overvoltage protection is necessary for most popular USB- or mini-USB-cable connections between adapters and portable devices. This feature improves safety by disabling the charger when the input voltage is above a safe voltage threshold. Once you remove the overvoltage, battery charging can resume. This

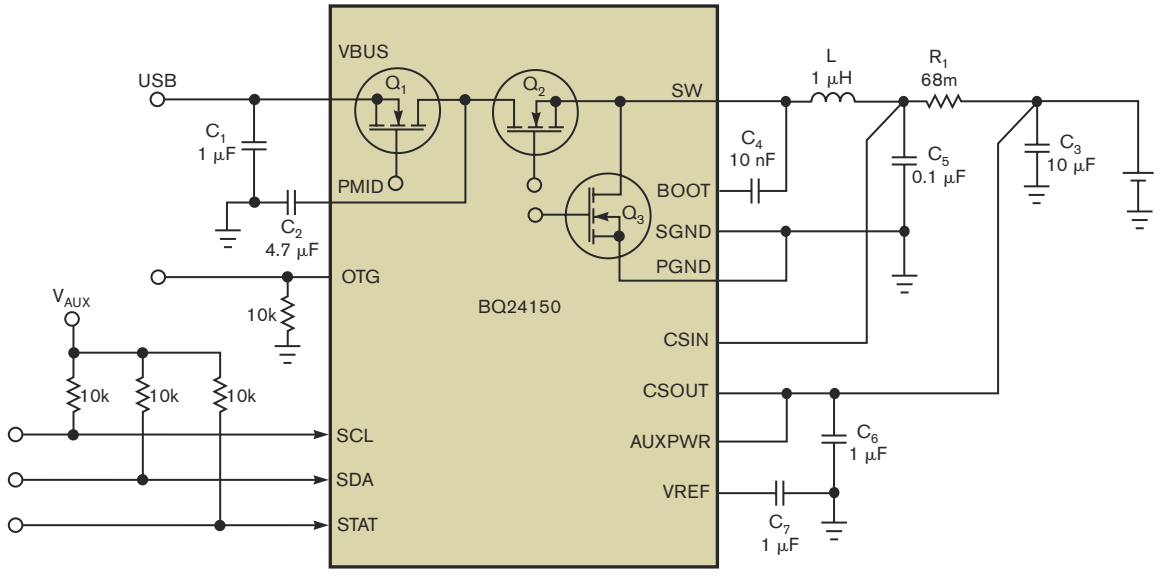

Figure 2 This 3-MHz synchronous-switching, step-down charger integrates power MOSFETs.

protection allows you to use adapters without damaging the charging system. A dynamic host-controlled safety timer starts a 32-minute timer that the host can stop with any write-action through the I^2C interface at the beginning of charging. Once the host stops the 32-minute timer, it automatically resets a 32-second timer by writing a one to the reset bit of the timer reset in the control register. This action causes the host to continuously start the 32-second timer to keep normal charging until charging terminates. If the 32-second timer expires because there is no writing action to the reset bit of the timer reset, the charging terminates, and the charge parameters reset to the default values. The 32-minute timer then restarts, and charging resumes.

During normal charging, a single-cell, synchronous-switch-mode charger, such as Texas Instruments' BQ24150, is in 32-second mode with host control and 32-minute mode without host control (**Reference 1**). The process repeats until the battery fully charges. If the 32-minute timer expires without a write command, it turns off the charger and announces a fault on the status register. This function prevents the battery from overcharging. Such dynamic host-controlled battery charging ensures that the battery is charging safely.

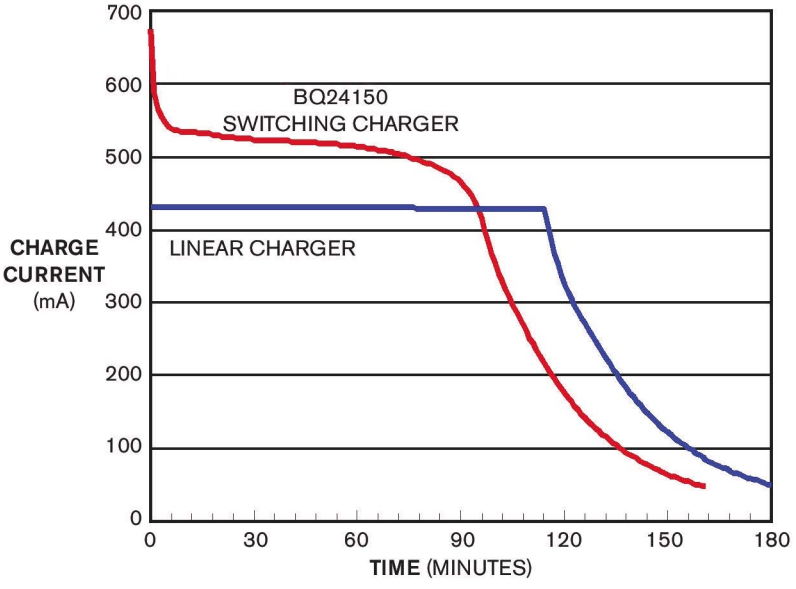

Figure 3 An experimental test-battery charge profile shows that the switch-mode charger can shorten the battery-charging time by more than 10%.

Thermal safety is another important consideration for integrated-power-MOSFET converters. One effective approach is to monitor and regulate the silicon-junction temperature in real time by introducing a thermal-regulation loop. You accomplish this task by reducing the charging current to control power dissipation and improve the thermal design so that the charger can operate safely.

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USB OTG SUPPORT

When you connect a portable device to a laptop computer through a USB port, you are automatically configuring the laptop as a host to provide 5V USB voltage for data communication. However, this configuration does not define the host for the communication between two portable slave devices—for example, sending the photos from a digital still camera to a cellular phone through a USB cable. USB OTG determines which system will be a host to provide 5V USB voltage from a lithium-ion battery. You cannot use a linear charger as a boost converter for this task.

You can use a synchronous-switching step-down converter as a bidirectional power converter, a synchronous boost converter, and a method of boosting the battery voltage to the 5V USB voltage to power another portable device in the USB port. For typical USB OTG applications, maximum output current of 200 mA is good enough for normal operation. High light-load efficiency is critical for extending battery runtime, which requires that the boost converter in USB OTG mode operates in PFM (pulse-frequency-modulation) mode to minimize switching losses. The typical application circuit in **Figure 2** operates in boost mode when you enable the USB OTG function. This feature enables support for the USB OTG specifications and facilitates communication between two slave portable devices.

The fully integrated, 3-MHz, synchronous-switching, step-down battery charger makes more efficient use of USB-port power, provides speedier charging for lithium-ion batteries, and provides 10% shorter USB charging time than does a linear-mode charger. The integrated loop compensator and 3-MHz switching frequency allow use of a chip inductor for minimizing the need for a number of external components. It also provides USB OTG support to allow communication between two slave mobile devices. EDN

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AUTHOR'S BIOGRAPHY

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Modern ADCs improve CMOS image sensors

IC DESIGNERS HAVE IMPROVED THE ADCs INSIDE CMOS SENSORS, WHICH MUST CAPTURE FRAMES QUICKLY ENOUGH FOR HIGH-DEFINITION VIDEO. WITH THIS CONSTRAINT IN MIND, DESIGNERS MUST WEIGH THE BENEFITS OF ADC ARCHITECTURES AND MAKE TRADE-OFFS IN SPEED AND SIZE.

The last two years have seen many important developments in CMOS image sensors using a variety of architectures that employ different methods to achieve similar goals. The ADCs that the image sensors employ are keys to these architectures, with manufacturers employing one of two major approaches: pipelined or column techniques. By studying devices from Samsung (www.samsung.com), Micron (www.micron.com), Sony (www.sony.com), Toshiba (www.toshiba.com), and STMicroelectronics (www.st.com), you can weigh the benefits of both types of ADC and decide which is best for your image-sensor application. As image sensors become more complex, they are using an increasing number of schematics in the analog paths (**Figure 1**). Large, stand-alone, pipelined ADCs are giving way to single-slope, integrating ADCs that align with the pixel array and contain an ADC for each col-

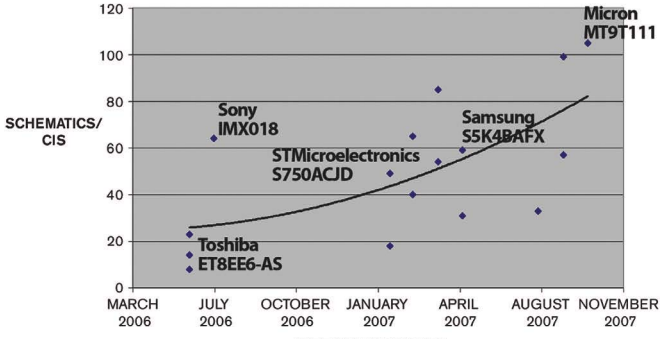

Figure 1 The number of schematics used to describe the analog paths of image sensors more than doubled in the last two years.

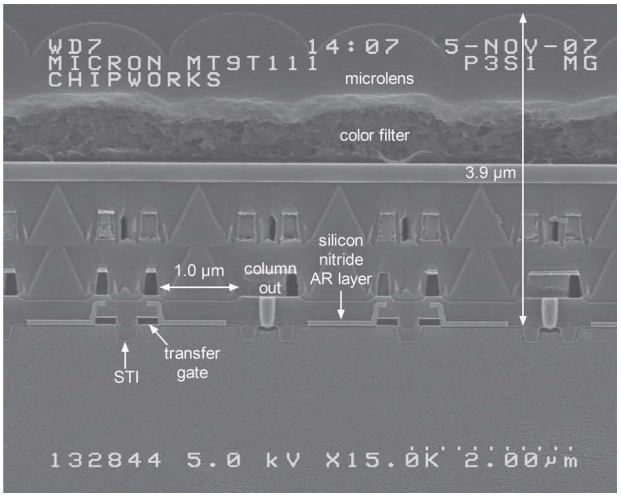

Figure 2 A SEM (scanning-electron-microscope) cross section shows the pixel array in a cell-phone image sensor.

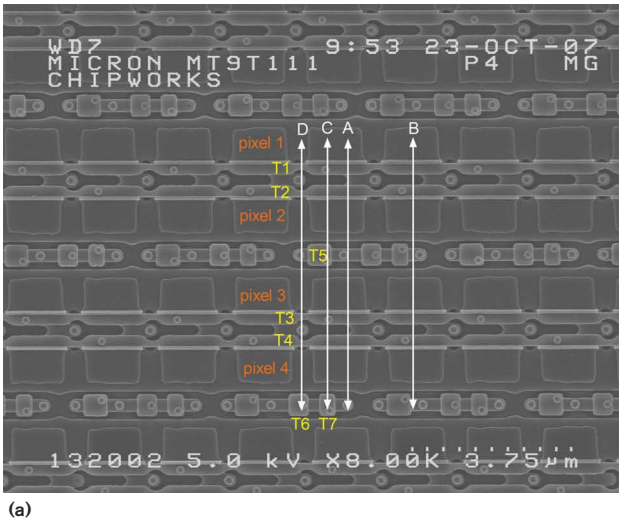

Figure 3 An image (a) and corresponding pixel schematic (b) show the 1.75T (transistor) architecture in the Micron MT9T111 CMOS image sensor. Lines A, B, C, and D represent a cross section for subsequent analysis.

umn of the array. The benefit of this approach is that it allows you to quickly move data off the sensor. Additionally, each ADC has a much longer time to operate on a sample, thus allowing longer settling times, lower noise, and higher accuracy.

Using imaging, software-based circuitry extraction, and schematic organization, you can take apart the layers of a CMOS sensor. The newest sensors combine the pixel array, ADCs, and digital-image processing on a die. They help to move light into the pixel, often in a noisy environment, and then move that data off the array. The sensors employ microlenses to help focus the light into the "light tube," which the readout circuitry's metal layers partially block (**Figure 2**). Because today's leading 1.4-micron pixel designs are bascially twice the wavelength of visible light, this task is difficult. To reduce circuitry, manufacturers often employ transistor-sharing techniques (**Figure 3**).

Circuit designers try to get as many dies onto a wafer as possible. In the CMOS-image-sensor world, especially for digital-single-lens-reflex cameras, designers must take into consideration the massive die necessary for capturing a 35-mm image. In that case, designers must concentrate on improving yield rather than saving area.

PIPELINED ADCs

Developers of the first CMOS image sensors modeled the devices on CCDs (charge-coupled devices), which preceded them. These early CMOS image sensors had an architecture similar to that of CCDs. In the next stage of CMOS-image-sensor evolution, designers brought pipelined ADCs on-chip. Pipelined architecture delivered the high bandwidth necessary for processing all the pixels of the array. Although these ADCs have long latencies, these delays are not problematic in this application. Early on-chip ADCs used a single simple pipelined design (**Figure 4**). These ADCs gradually evolved to the current state-of-the-art DDR (double-data-rate), fully differential, multiple-pipelined ADCs. The analog-signal path from the light-collecting photodiode to the ADC is now fairly standard across the industry. The chip electronics must select a single

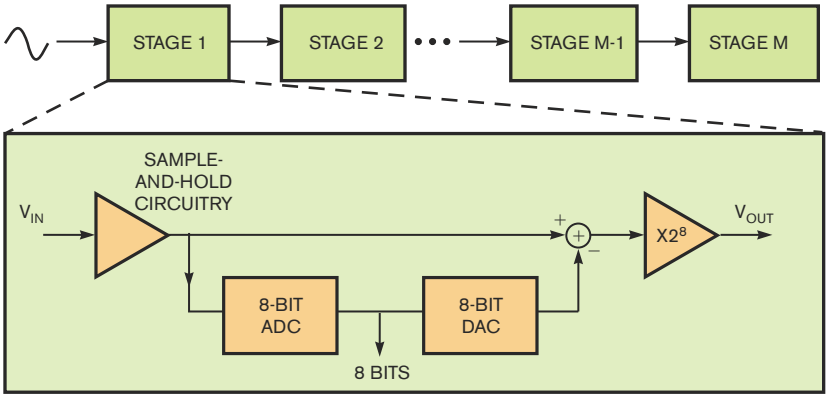

Figure 4 A pipelined-ADC architecture consists of repeated stages.

row of pixels, transfer the signals to column circuits, perform correlated double sampling, and then sample and hold the resultant signals.

Many manufacturers now use this architecture to reduce the number of transistors in the array. The Micron MT9T111 1.75T, for example, employs seven transistors and four photodiodes (**Figure 3**). When system electronics activate the row-select signal, the chip connects the selected row of pixels to the column-out line. These signals travel to the edge of the array in which the pitch-matched column-parallel-sampling circuits reside. The signal typically first reaches a multiplexer, allowing multiple columns of pixels to use the same analog-processing column. This approach also allows the selection of only a subset of pixels during high-speed image capture for preview and downscaling, or "binning." Active loads are also present at this point to bias and clamp the signals.

The image signals then enter the correlated-double-sampling circuit (**Figure 5**). Metal layers shade some photodi-

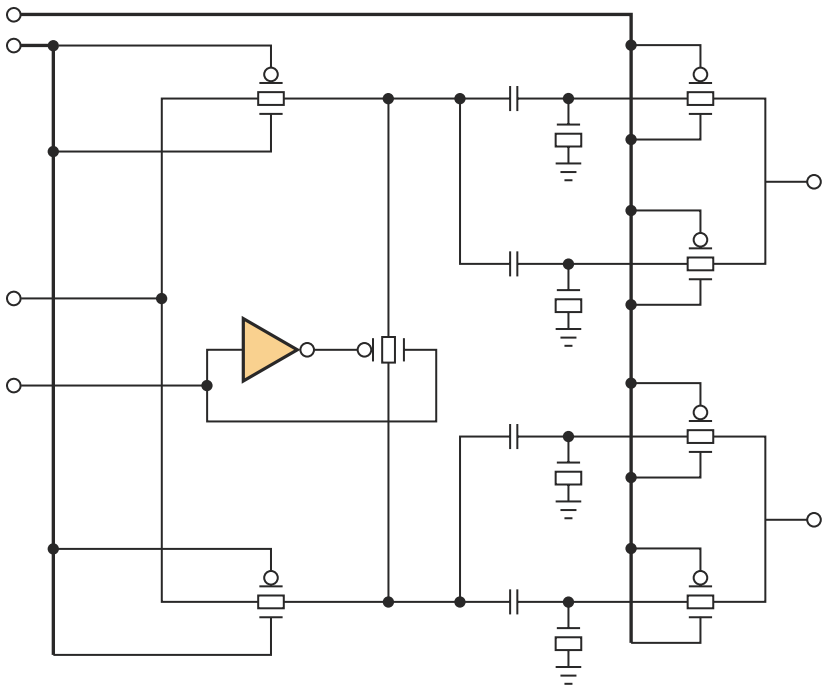

Figure 5 The Micron MT9E001 uses a modern correlated-double-sampler design.

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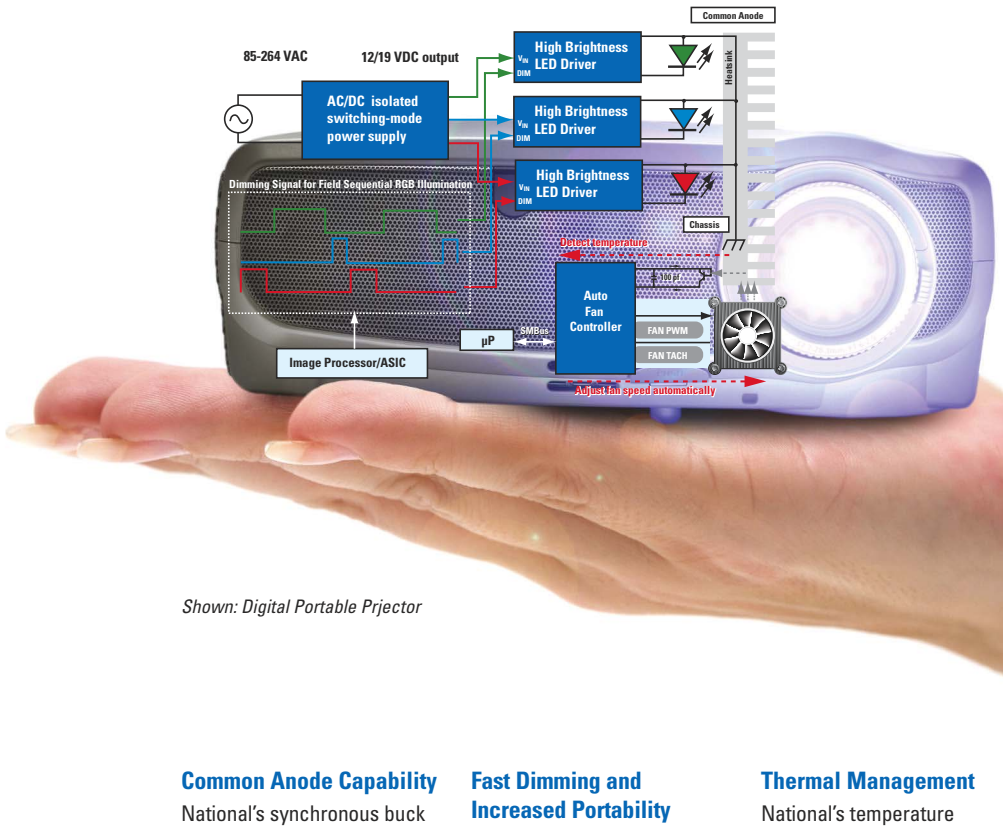

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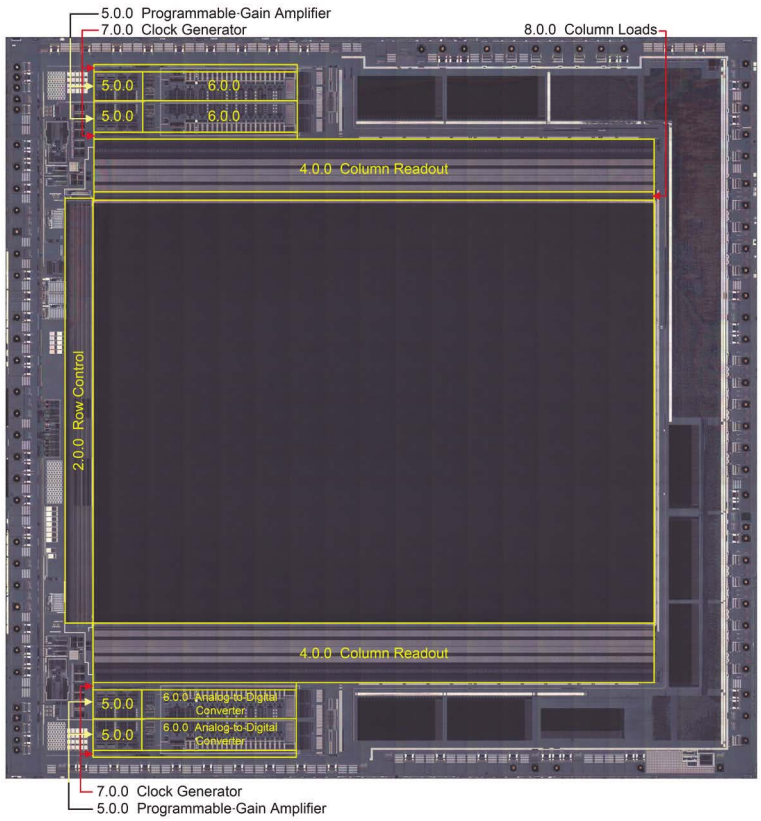

Figure 6 The Micron MT9E001 uses four pipelined ADCs.

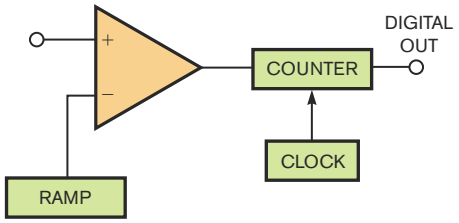

Figure 7 The single-slope integrating-column ADC finds use in most CMOS image sensors.

odes, which the circuitry reads to establish the black levels along the row. Next, the circuitry samples the actual data signal and subtracts the black level to give the output level. At this point, the pipelined ADC architecture multiplexes the signals from the pitch-matched column circuits to the ADCs. As speed and bandwidth requirements have increased, IC designers have added more ADCs. For example, the Micron MT9E001 for digital cameras uses four 12-bit ADCs (**Figure 6**).

Both the MT9E001 and the MT9T111 use a DDR, fully differential-pipelined scheme. The parts can achieve a 96-Mbps data rate at 400-mW power consumption. One feature of the DDR scheme is that dual-pipelined ADCs share the operational amplifier, allowing the chip to acquire two samples and perform two conversions in one clock cycle. No dc-bias current goes unused during the sampling phase of the operation. A key disadvantage of this architecture is layout difficulty (**Reference 1**). However, capacitor matching in this device is adequate for achieving 12 bits of accuracy without digital correction (**Reference 2**). The four DDR, 12-bit pipelined ADCs on the chip make it possible for the MT9E001 to exceed the speed of CCDs.

COLUMN ADCs

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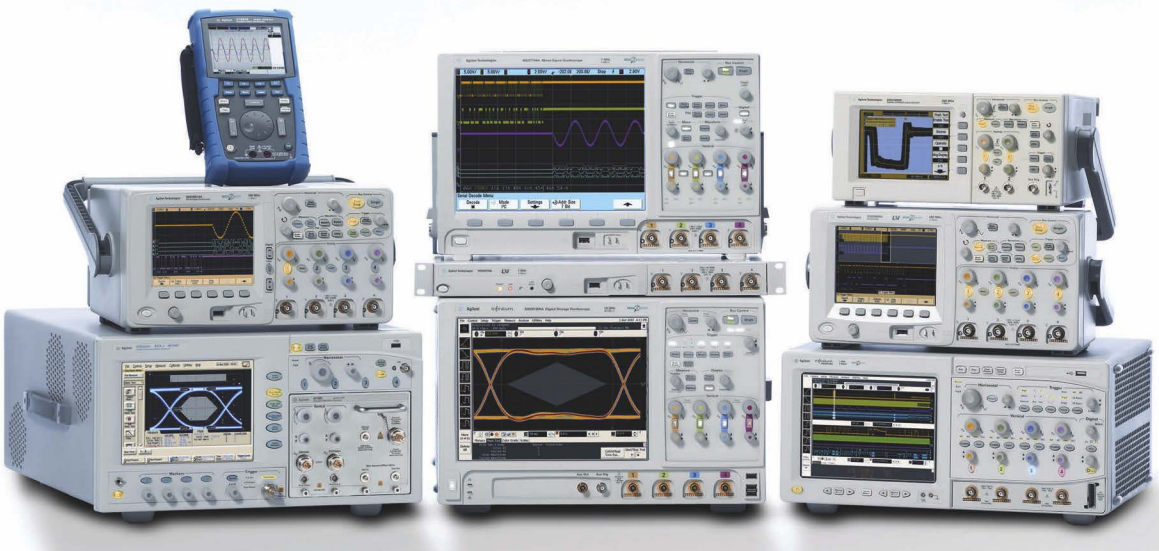

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times, making it difficult to quickly take a series of consecutive pictures. To address that problem, manufacturers developed column-parallel ADCs, which allow the CMOS sensor to take pictures at 60 frames/sec in the pitch-matched column area. For example, the 2M-pixel Samsung S5K4BAFX CMOS image sensor for cell-phone cameras has 882 parallel ADCs. In this design, the ADCs are small and the speed-per-ADC requirement is low. Column-parallel ADCs use single-slope integrating-ADC architectures (**Figure 7**). Only the comparator and the counter need to be in the column pitch. The devices can generate the ramp-reference signals and clocks outside the column, and all the ADCs can share these signals and clocks. As in the pipelined-ADC architecture, column ADCs multiplex the signal and then apply active loads. The usual correlated double sampling then takes place.

At this point in the signal path, the designs diverge. In the column-parallel-ADC architecture, the pixel signal goes to one input of a comparator, in which the other input is a ramp voltage. The output of this comparator acts as the enable signal to a counter. This counter synchronizes with a master counter to create the ramp signal. When the ramp voltage exceeds the pixel voltage, the comparator flips, and the counter becomes disabled. The counter then holds the digital value corresponding to the analog pixel voltage on 882 columns in parallel.

This architecture allows for small and simple ADCs in the column pitch and moves the accuracy and speed constraints to the ramp generator. This ramp generator must now accurately and quickly convert a digital value that a counter creates to an analog voltage to act as the ramp. Because the S5K4-BAFX has a 10-bit ADC, the ramp-generator DAC must accomplish 1024 conversions for the 882 ADCs to convert their value at a faster rate than one ADC could operate. To accomplish this task, the first 10-bit column-parallel ADCs employed flash DACs using resistor dividers as the ramp generator. The Samsung S5K4BAFX has a subranging resistor divider, a coarse voltage divider of 16 resistors, a fine voltage divider of 16 resistors, and an LSB-resistor string of four resistors, resulting in the required 1024 levels (**Figure 8**).

NEXT-GENERATION ADCs

Samsung was the first manufacturer to introduce an advanced column ADC. In 2007, the company released the S5K4C1GX 3Mp CMOS image sensor, employing a 12-bit ADC, for mobile phones. Samsung manufactured the device in a 90-nm process, and it uses a similar single-slope integrating-column ADC as in the previous generation, including a comparator and a 13-bit counter. The 13 bits allow for a full

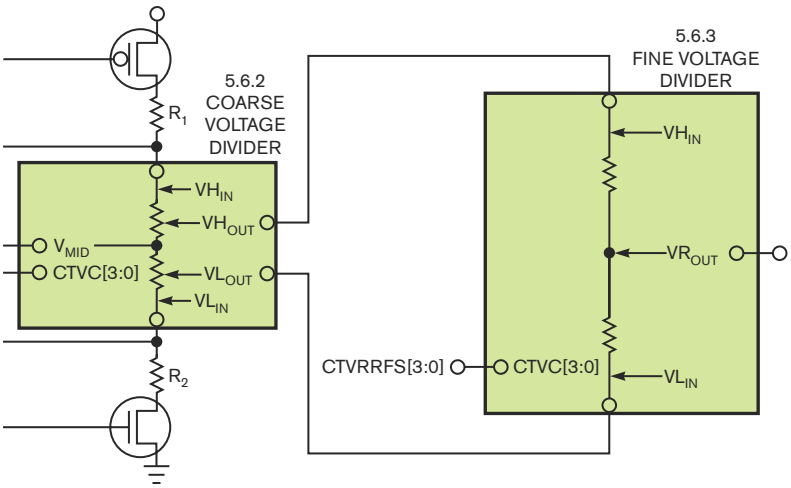

Figure 8 The Samsung S5K4BAFX resistor-divider ramp generator can generate 1024 levels.

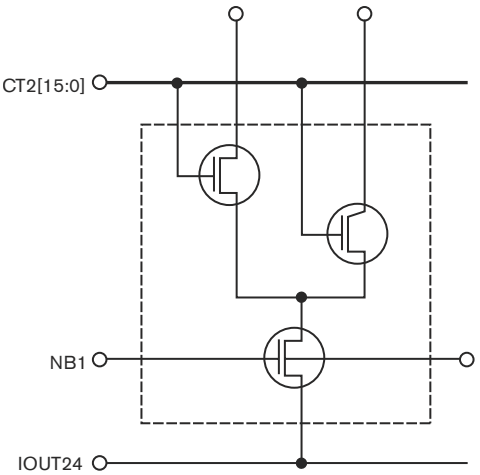

Figure 9 The Samsung S5K4C1GX current-steering DAC cell replaces previous resistor-string designs.

12-bit value plus overflow. The part's ramp generator uses a current-steering DAC to replace the resistor-string DAC of the previous generation (**Figure 9**). This innovation is significant because current-steering DACs are more complex and occupy more area. For a 12-bit ADC, the need for precision in the reference voltage is great enough to require the complexity and additional space of the current-steering DAC. Samsung uses three current-steering arrays and combines their outputs in a fourth array. Each array is a stand-alone current-steering DAC, including an array of unity-current sources and their respective steering transistors. A fully decoded 13-bit counter drives the array.

Sony in 2007 announced its first CMOS image sensor employing a column ADC; the company's previous sensors employed pipelined ADCs. Today, three Sony CMOS image sensors—one for mobile phones, one for digital-single-lens-reflex cameras, and one for camcorders—use column ADCs. Surprisingly, the design is not specific to high-frame-rate applications. Sony has taken this architecture one step further in the IMX017 camcorder CMOS-image sensor. The device uses a digital, rather than analog, correlated-double sampling circuit. Rather than storing the black pixel voltages on a capacitor for later subtraction from the signal, the device samples the black pixels directly on the ADC comparator. The device then compares these black signals with the ramp voltage, and the counter counts down during this phase until the ramp voltage crosses the black signal and the counter stops. The unit then applies the pixel voltage to the comparator, and the counter starts counting up, effectively subtracting the black signal from the pixel value. This digital architecture eliminates the need for large sampling capacitors and reduces switching noise.

CMOS-image-sensor commercialization has been rapid. One or two players do not dominate the market. The result is a range of innovation, as the small but important ADC demonstrates. Expect market convergence within the next three to five years. Meanwhile, tracking the major designs will be interesting. EDN

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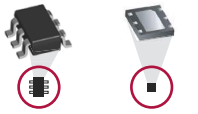


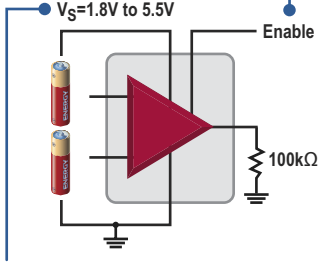
Actual Size (2.6x2.8mm) | Actual Size (1.6x1.6mm)

Other Members of Intersil's Nanopower Family

Device	I_{SS}/Amp (typ)	Function
ISL28194	330nA	Op Amp
ISL28195	1µA	Op Amp
ISL28196	2.5µA	Comparator
ISL28197	800nA	Comparator
ISL60002	400nA	Voltage Reference
X60003	500nA	Voltage Reference

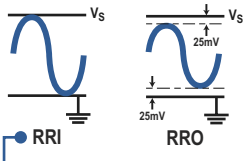
Extended Battery Life:

1. Consumes less current during operation.
2. Consumes only 2nA when amplifier is disabled.



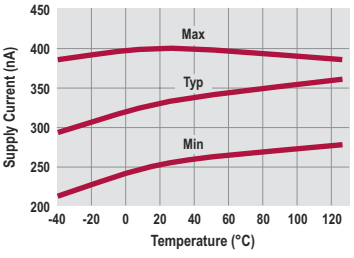
Rail-to-Rail Input/Output

Allows full dynamic range and maximum battery usage.



3. Designed for single-supply operation from 1.8V to 5.5V and ideal for low-power precision applications that run on 1.5V alkaline batteries.
4. True rail-to-rail input simplifes system design and supports maximum signal levels.

ISL28194



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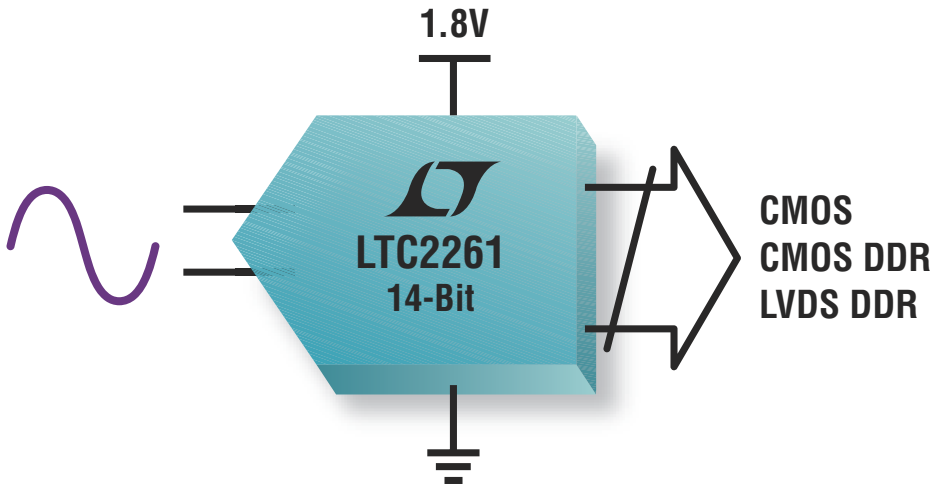

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- Optional Data Output Randomizer
- Shutdown (0.5mW) and Nap (9mW) Modes
- 40-Pin (6mm x 6mm) QFN Package

Lowest Power ADC Family

Part Number	Speed	Power	SNR
LTC2261-14	125Msps	125mW	73.4dB
LTC2260-14	105Msps	106mW	73.4dB
LTC2259-14	80Msps	89mW	73.4dB
LTC2261-12	125Msps	125mW	70.8dB
LTC2260-12	105Msps	106mW	70.8dB
LTC2259-12	80Msps	89mW	70.8dB

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EDITED BY MARTIN ROWE
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designideas

READERS SOLVE DESIGN PROBLEMS

Increase the range of memorized voltage for a sample-and-hold device

Yakov Velikson, Lexington, MA

Sample-and-hold devices find use in front of ADCs. The basic sample-and-hold circuit comprises two op amps, A_1 and A_2; a switch, S_1; and a capacitor, C_1 (**Figure 1**). For many low-power op amps, the values of the input and output voltages can be only ±10 to ±14V using a standard ±15V power supply. Enabling these devices to handle greater voltage can significantly improve the resolution of an ADC.

You can increase the memorized voltage that amplifiers A_1 and A_2 can reach by using a variable power supply (**references 1** and **2**). This approach places additional voltage requirements on S_1, however. To continue using switches with the same range as the original, you must add two switches and independent control-logic blocks, CL_1 and CL_2, for switches S_1, S_2, and S_3 (**Figure 2**). The two parts of the circuit may have independent power supplies. You apply the same variable voltages to amplifiers A_1 and A_2 as you do to control-logic blocks CL_1 and CL_2, respectively. When S_1 and S_3 are closed, S_2 is open, and vice versa.

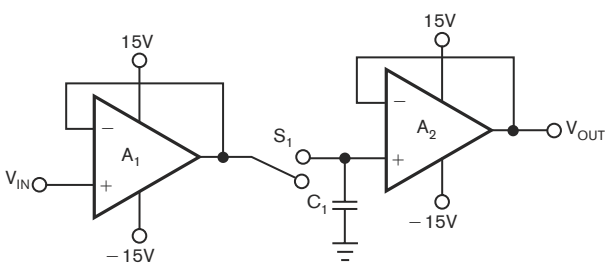

Figure 1 A basic sample-and-hold circuit comprises two op amps, a switch, and a capacitor.

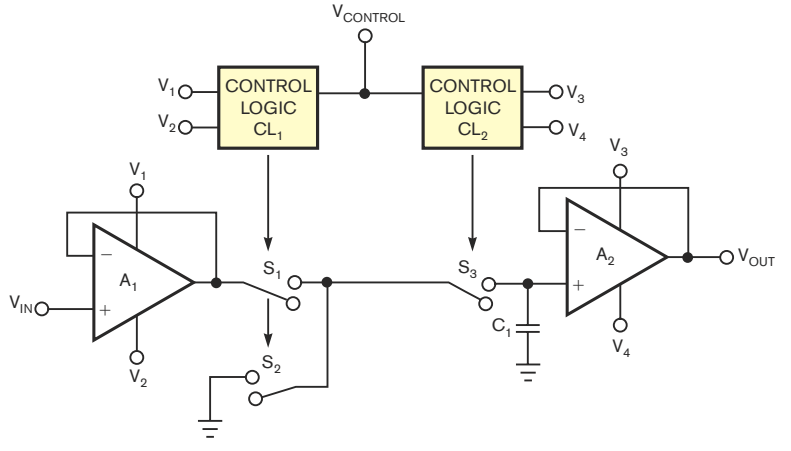

Figure 2 To continue using switches with the same voltage range as that of Figure 1, you must add two switches and two independent control-logic blocks.

The resulting circuit keeps the voltages connected to the gate and substrate for the MOS transistors of each switch within the desired 30V range (**Figure 3**). (You derive this value from the sum of absolute-voltage values: $|V_1|+|V_2|$ and $|V_3|=|V_4|$.) Voltages V_1 and $-V_2$ connect to amplifier A_1, control-logic block CL_1, and the substrates of the transistors of switches S_1 and S_2. Voltages V_3 and $-V_4$ connect to amplifier A_2, control-logic block CL_2, and the substrates of the transistors of switch S_3.

You create the changing voltages of V_1 and V_2 using resistor dividers R_5 and R_6 and R_7 and R_8, which connect to the 30 and the −30V power supplies and the output of amplifier follower A_1 (**Figure 3**). Transistors Q_1 and Q_2 create the change to the power supply of amplifier A_1. Volt-

DIs Inside

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ages V_1 and V_2 also supply power to control-logic block CL_1 and the substrates of the transistors of switches S_1 and S_2. CL_1 comprises transistors Q_{11}, Q_{12}, Q_{15}, and Q_{16}. It creates a control signal for gates Q_5 and Q_6 of switch S_1 and the inverse signal for gates Q_8 and Q_9 of S_2.

Resistor dividers R_9 and R_{10} and R_{11} and R_{12} connect to the 30 and the −30V power supplies, and the output of amplifier follower A_2 creates the changing voltages V_3 and V_4. Transistors Q_3 and Q_4 create the change to the power supply of amplifier A_2. Voltages V_3 and V_4 also supply power to control-logic block CL_2 and the substrates of the transistors of switch S_3. CL_2 is made up of transistors Q_{13}, Q_{14}, Q_{17}, and Q_{18}. It creates a control signal for gates Q_7 and Q_{10} of switch S_3. Transistors Q_5 through Q_{10} and Q_{11} through Q_{18} of CL_1 and CL_2, respectively, are complementary pairs of MOS logic transistors. EDN

REFERENCES

1 Velikson, Yakov, "Controlled power supply increases op amp's output-voltage range," *EDN*, March 15, 2007, pg 72, www.edn.com/article/CA6421438.

2 Velikson, Yakov, and Igor Ribkin, "Analog switch, 1385288," *Bulletin of Izobreteny (Copyrights and Patents)*, No. 12, 1988.

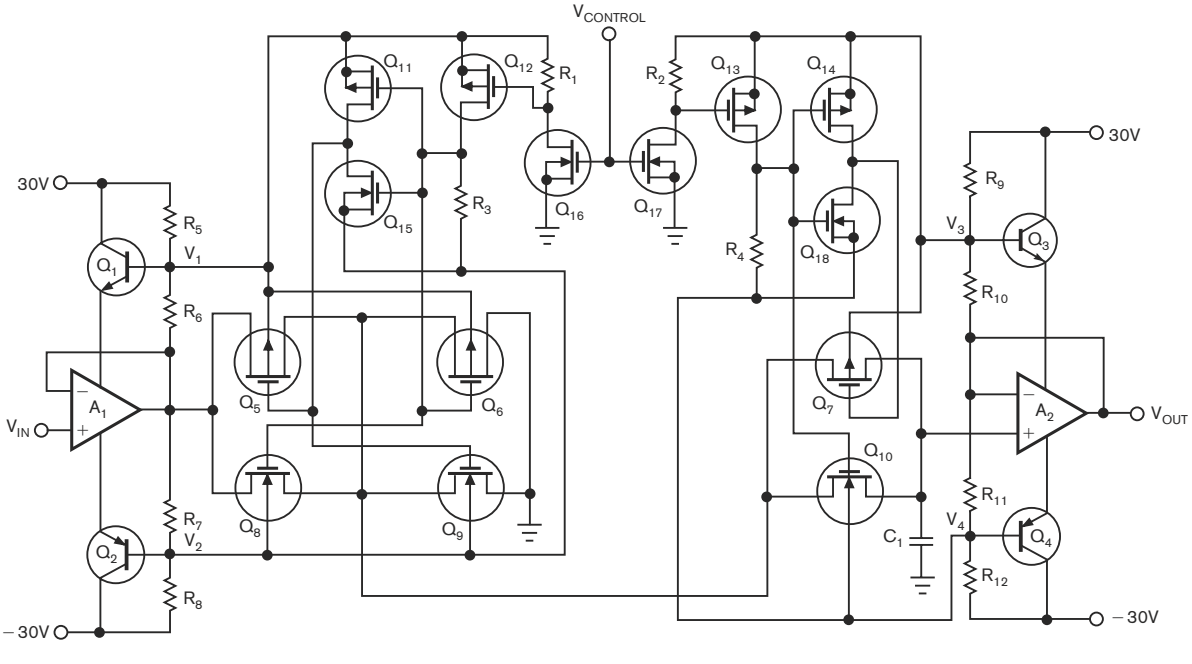

Figure 3 You can create the changing voltages of V_1 and V_2 using resistor dividers R_5 and R_6 and R_7 and R_8.

Inexpensive self-resetting circuit breaker requires few parts

Anthony H Smith, Scitech, Bedfordshire, England

Most readers are familiar with the current-limiting circuit in **Figure 1**, in which the load current, I_L, is limited to a value of $I_L \approx V_{BE}/R_S$, where V_{BE} is the base-to-emitter voltage and R_S is the sense resistance. Under normal conditions, in which the base-to-emitter voltage is too small to bias Q_1 on, P-channel MOSFET Q_2's gate resistor, R_G, biases Q_2 fully on, and only the load resistance, R_L, and the load voltage, V_L, determine the load current. However, if the load current increases to a point at which the base-to-emitter voltage is approximately 0.7V, Q_1 starts to conduct and reduces Q_2's gate-to-source voltage, V_{GS}, to a level that holds the load current roughly constant at a value you derive from $I_{LMAXIMUM} \approx 0.7V/R_S$.

This linear current limiter is effective for applications in which the maximum load current, the supply voltage, or both are relatively small. However, the power that the circuit's pass transistor, Q_2, dissipates limits the circuit's applicability. For example, if the maximum load current is 200 mA and the supply voltage, V_S, is 24V, a short circuit across the load would dissipate almost 5W into Q_2. Q_2 must handle this power with adequate margin, and additional heat-sinking may be necessary to keep its junction temperature at a safe level. Using larger values of

DESIGN NOTES

Monolithic Synchronous Step-Down Regulator Delivers up to 12A from a Wide Input Voltage Range – Design Note 457

Charlie Zhao and Henry Zhang

Introduction

The LTC®3610 is a high power monolithic synchronous step-down DC/DC regulator that can deliver up to 12A of continuous output current from a 4V to 24V (28V maximum) input supply. It is a member of a high current monolithic regulator family (see Table 1) that features integrated low $R_{DS(ON)}$ N-channel top and bottom MOSFETs. This results in a high efficiency and high power density solution with few external components. This regulator family uses a constant on-time valley current mode architecture that is capable of operating at very low duty cycles at high frequency and with very fast transient response. All are available in low profile (0.9mm max) QFN packages.

Table 1. Comparison of LTC36XX Family Members

	LTC3608	LTC3609	LTC3610	LTC3611
INPUT VOLTAGE RANGE (V)	4 to 20	4.5 to 32	4 to 24	4.5 to 32
MAX LOAD CURRENT (A)	8	6	12	10
QFN PACKAGE SIZE (mm)	7 × 8 × 0.9	7 × 8 × 0.9	9 × 9 × 0.9	9 × 9 × 0.9

Typical Application Example

Figure 1 shows a typical application schematic of the LTC3608. This 7mm × 8mm regulator supplies 2.5V at 8A maximum load current from a 4.5V to 20V input source. This application switches at a nominal 650kHz, which allows the use of low profile inductor and capacitors while maintaining high efficiency. The switching frequency can be easily adjusted by a resistor (R_{ON} in Figure 1, connected to the I_{ON} pin). Figure 2 shows the operating efficiency.

The FCB pin is connected to ground to force continuous mode operation at light load for both low noise and small output ripple. The FCB pin can also be tied to $INTV_{CC}$ to enable discontinuous mode for higher efficiency at light load. Soft-start is programmable with a capacitor from the RUN/SS pin to ground. Forcing the RUN/SS pin below 0.8V shuts down the device.

The LTC36XX family are valley current mode regulators so they inherently limit the cycle-by-cycle

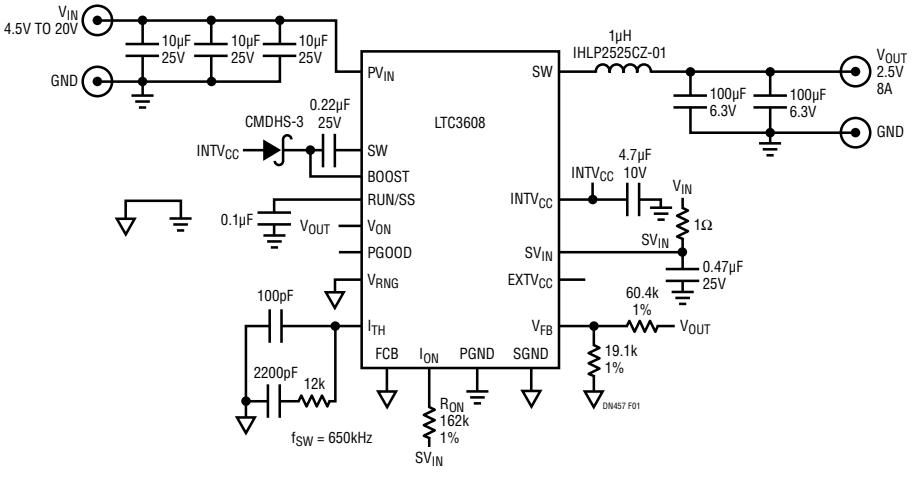

Figure 1. 4.5V to 20V Input to 2.5V/8A High Density Step-Down Converter

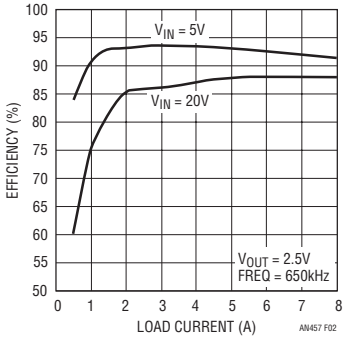

Figure 2. Efficiency vs Load Current of Figure 1

inductor current. The inductor current is sensed using the $R_{DS(ON)}$ of the bottom MOSFET —no additional current sense resistor is required. The current limit is also adjustable with the voltage at the V_{RNG} pin. When the V_{RNG} pin is tied to ground, in the Figure 1 example, the current limit is set to about 16A.

An open-drain logic power good output voltage monitor (PGOOD) is pulled low when the output voltage is outside ±10% of the regulation point. In the case of overvoltage, the internal top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition clears. The LTC36XX also includes a foldback current limiting feature to further limit current in the event of a short circuit. If the output drops more than 25%, the maximum sense voltage is lowered to about one sixth of its original value.

Paralleling Regulators for >12A

These parts can be easily paralleled for high output current applications. Figure 3 shows a 1.2V/24A application using two parallel LTC3610s. Because of the valley current mode control architecture, the paralleled regulators can operate at very low duty cycles with fast transient response and excellent load balance.

The current sharing is simple. Connect the I_{TH} pins together, since the I_{TH} pin voltage determines the cycle-by-cycle valley inductor current. The feedback pins of paralleled LTC3610s share a single voltage divider. The RUN/SS pins are connected so that the LTC3610s start up with same slew rate. The paralleled LTC3610s have excellent thermal balance due to good current sharing.

Conclusion

With broad input and output ranges, high current capability and high efficiency, these monolithic regulators provide small size, low external component count power solutions for many applications from communications infrastructure to industrial distributed power systems.

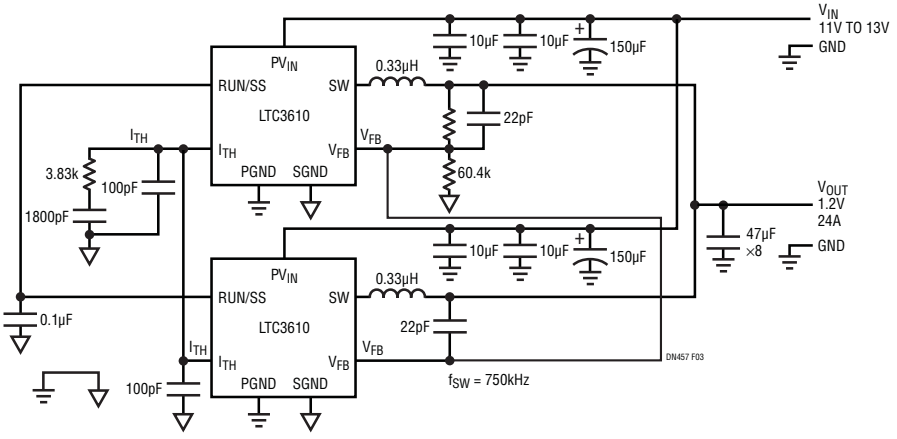

Figure 3. Two LTC3610s in Parallel Can Provide 24A Output Current

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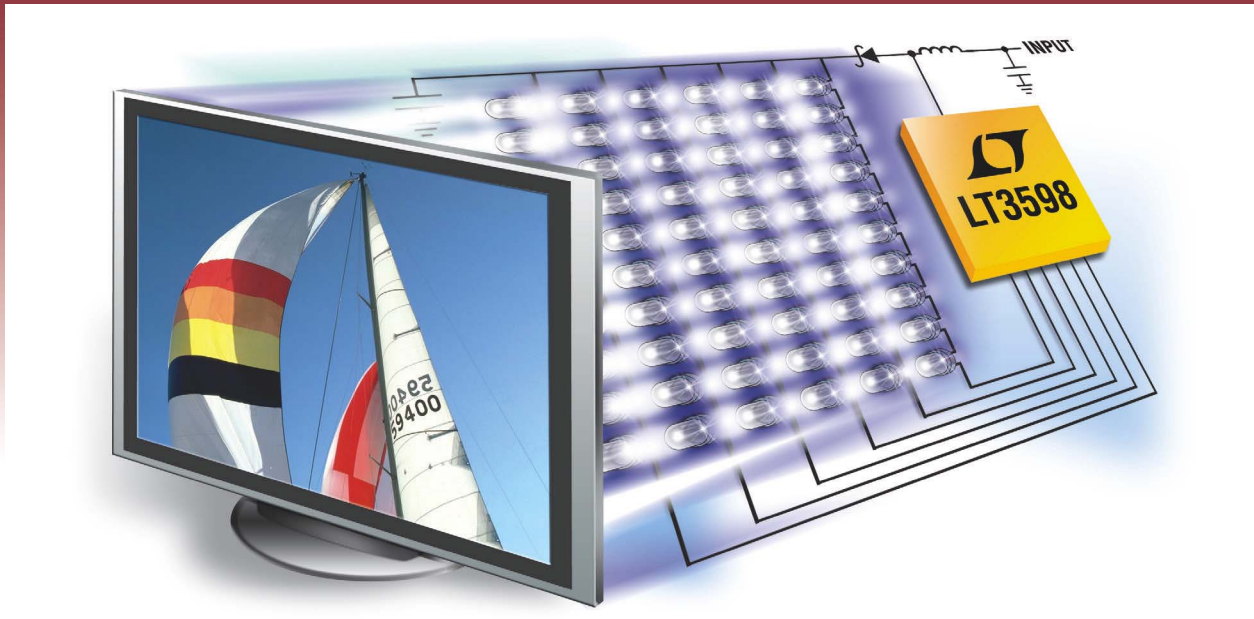

36V_{IN}, 2.5MHz, 3000:1 PWM Dimming Range LED Driver

Many small to medium-size panel displays need large numbers of white LEDs for backlighting. Powering and driving up to 16W for these LEDs is challenging due to size and thermal constraints. With the LT®3598 and LT3599, the solution just got easier. These multiple-string LED drivers deliver up to 16W (7W for LT3598) of power and allow a 3000:1 dimming range for brightness adjustment, high LED current accuracy for uniformity of light output, good thermal and LED protection features for a rugged, compact design.

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LT3598 Demo Circuit

Actual Size

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maximum load current, supply voltage, or both exacerbates this problem. In many applications, the cost, size, and weight of the components necessary to handle the short-circuit power dissipation may be prohibitive.

However, by adding a few inexpensive components, you can adapt the circuit to provide effective current limiting with none of the power-dissipation headaches. The resulting circuit functions as a self-resetting circuit breaker (**Figure 2a**). Again, Q_1 and R_S provide a current-monitoring function in which the sense voltage $V_{SENSE}=I_L \times R_S$. In this circuit, however, Q_2 is either fully on or fully off and never biases into its linear region. Because Q_1's base current is normally small, the voltage drop across base resistor R_B is also small, such that the base-to-emitter voltage is approximately equal to the sense voltage.

To understand how the circuit works, assume that the load current is initially low and the base-to-emitter voltage is less than 0.7V. Under these conditions, Q_1 is off and timing capacitor C_1 remains uncharged such that V_{IN}, the voltage at the input of Schmitt inverter IC_1, is 0V. Thus, IC_1's output is approximately 5V, biasing Q_3 on, which in turn provides gate bias for Q_2 through R_4, allowing current to flow from the supply voltage into the load through the sense resistor and Q_2's on-resistance.

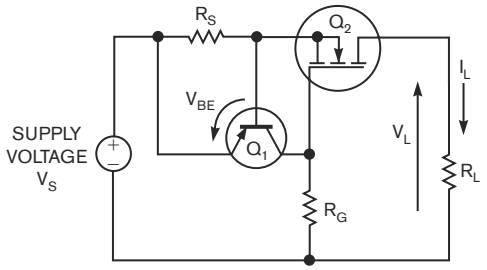

Figure 1 A conventional two-transistor current limiter prevents excessive current from reaching the load.

If a fault now causes the load current to increase to a level at which the base-to-emitter voltage is approximately 0.7V, Q_1 turns on and its collector current rapidly charges C_1. The input voltage now quickly rises toward the Schmitt inverter's upper threshold voltage, V_{TU}, at which point IC_1's output goes low, turning off Q_3 and Q_2. The load current now falls to 0A and the base-to-emitter voltage falls to 0V, thereby causing Q_1 to turn off. C_1 now begins to discharge through R_1 and R_2, and the input voltage slowly falls toward the Schmitt inverter's lower threshold voltage, V_{TL}. At this point, IC_1's output again goes high, Q_3 and Q_2 turn on, the circuit breaker resets itself, and the process repeats until you remove the fault.

The circuit's waveforms show the relationship between the input voltage and the load voltage (**Figure 2b**). Because load current flows into Q_2 only during the on-time, the average power it dissipates is directly proportional to the duty cycle: $P_{AVG} \propto t_{ON}/(t_{ON}+t_{OFF})$, where P_{AVG} is the average power in watts, t_{ON} is the on-time, and t_{OFF} is the off-time. Provided that C_1, R_1, and R_2 set a large enough time constant, the off-time will normally be much greater than the on-time, and the resulting power that Q_2 dissipates will be low. Like the linear-current limiter, the sense resistor sets the circuit breaker's current limit: $I_{LMAXIMUM} \approx 0.7V/R_S$ (A).

R_1 and R_2 form a potential divider that ensures that the input voltage can never exceed IC_1's maximum input voltage. Select values such that the input voltage is 5V or less when Q_1 is fully on, where the voltage of C_1 is roughly equal to the supply voltage. Also, choose values that are large enough to provide a large time constant without requiring an excessively large value of C_1. The selection of transistor Q_1 isn't critical, but you should select a device with good current gain and make sure that its maximum collector-to-emitter voltage is greater than the supply voltage. When choosing a P-channel MOSFET for Q_2, re-

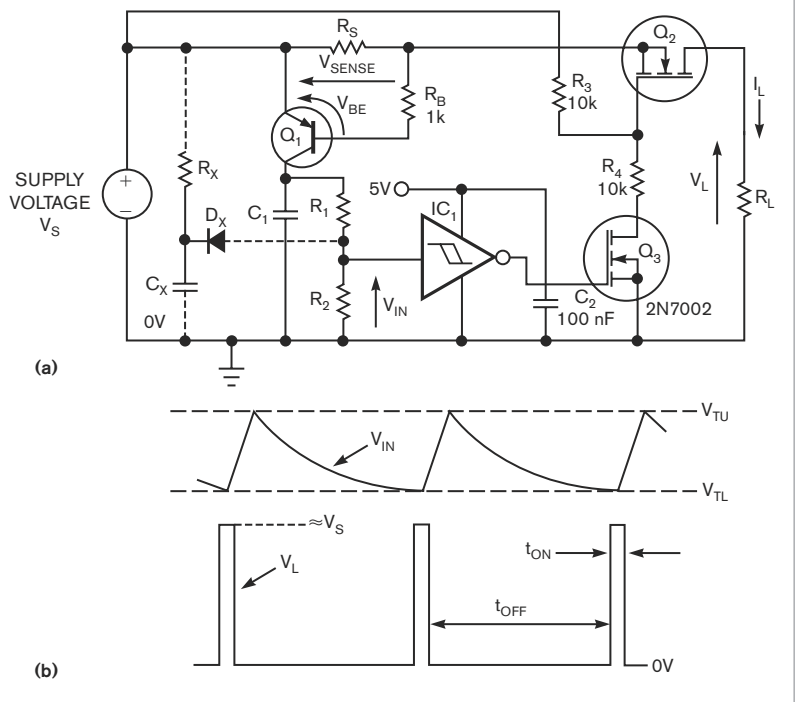

Figure 2 Adding a few components turns the current-limiting circuit into a pulser that reduces heat in the pass transistor, Q_2 (a). The circuit's waveforms show the relationship between the input voltage and the load voltage (b).

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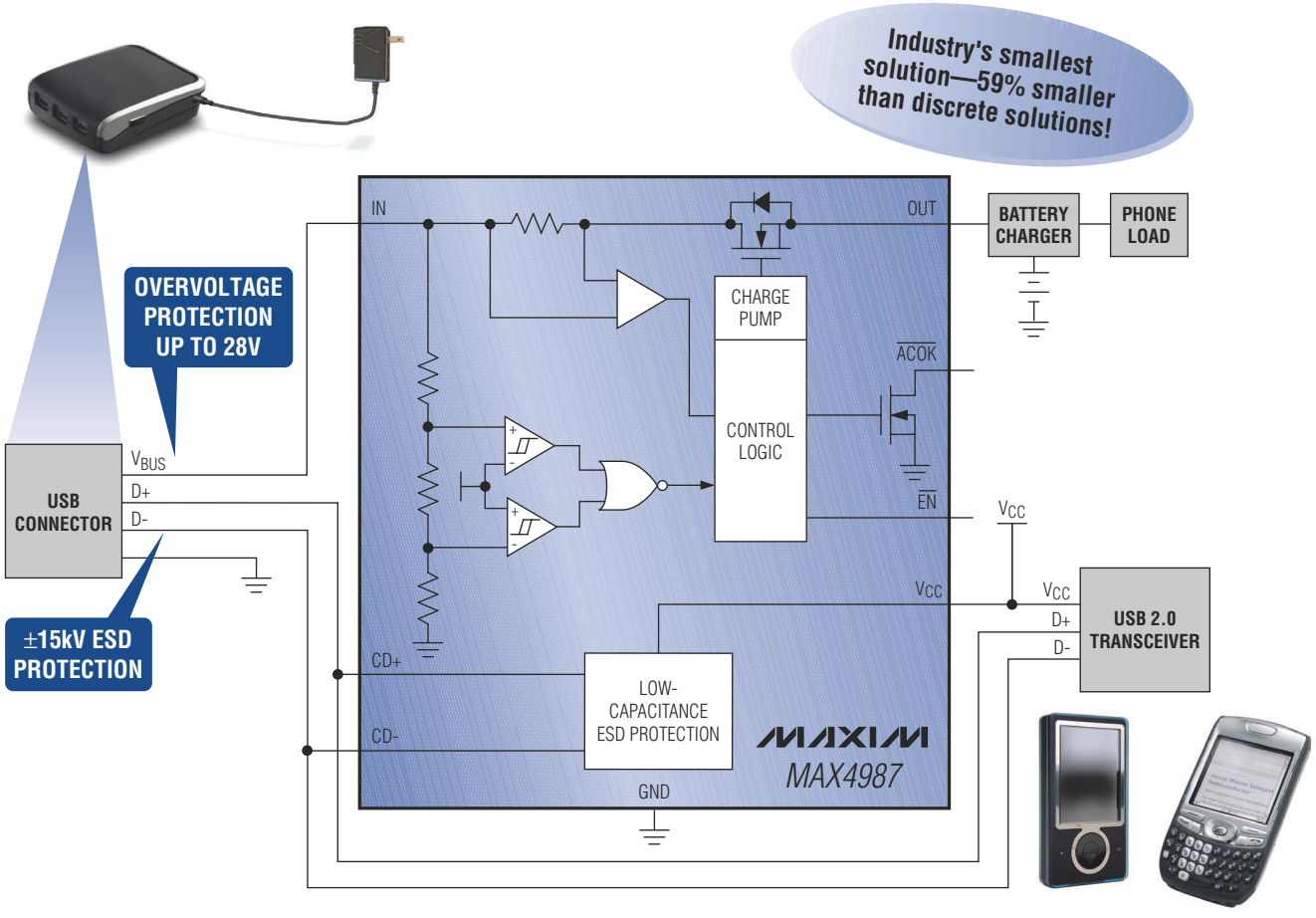

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member that it must withstand the full supply voltage when you bias it off, so make sure that the maximum drain-to-source voltage is greater than the supply voltage. When choosing a value for the sense resistor, ensure that the base-to-emitter voltage is less than 0.5V at the maximum normal value of the load current.

Loads such as filament bulbs, capacitive loads, and motors that exhibit a large inrush current can cause the circuit breaker to trip on power-up. You can avoid these problems by adding capacitor C_X, diode D_X, and resistor R_X. On power-up, C_X is initially uncharged and pulls the input voltage toward 0V through D_X. This action prevents the circuit breaker from tripping until the inrush current subsides. C_X and R_X determine a delay, after which the voltage on C_X eventually rises to the supply voltage, D_X becomes reverse biased, and the circuit breaker is then free to respond to overcurrent faults. Be prepared to experiment with the values of C_X and R_X to get the right delay time. Values of 10 µF and 1 MΩ, respectively, are good starting points. EDN

Sinusoid generator uses dual-output current-controlled conveyors

Abhirup Lahiri, Netaji Subhas Institute of Technology, New Delhi, India

Second-generation current conveyors feature wide signal bandwidth, linearity, wide dynamic range, simple circuitry, and low power consumption. Hence, designers employ several implementations of current mode in these devices for realizing various functions. A previous Design Idea introduced a second-generation dual-output current-controlled conveyor to create oscillators (**Reference 1**). Unfortunately, these circuits aren't available as ICs, but you build them from discrete components. **Figure 1** illustrates an active building block of such a circuit, which the following **equations** characterize: $I_Y=0$, $V_X=V_Y+I_XR_X$, $I_{Z+}=I_X$, and $I_{Z-}=-I_X$. You can express the parasitic resistance at terminal X as $R_X=V_T/2I_B$, where V_T is the thermal voltage and I_B is the bias current of the conveyor that is tunable over several decades. **Figure 2** shows the bipolar implementation of the circuit.

The circuit provides an extra degree of freedom in the sense that the control over the frequency of oscillation can be through both current and voltage. The circuit in the previous Design Idea provides various advantages, it this new circuit not only retains all those essential advantages, it also provides an extra feature of voltage controllability of frequency of oscillation.

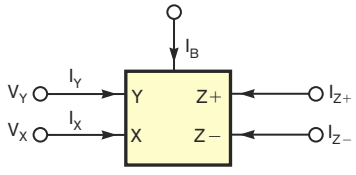

Figure 1 Second-generation current conveyors feature wide signal bandwidth, linearity, wide dynamic range, simple circuitry, and low power consumption.

Additionally, you can control the condition of oscillation using the conveyors' bias currents.

Figure 3 shows the proposed sinusoid-oscillator circuit. You can obtain the characteristic **equation** for the circuits as follows: $S_2C_1C_2R_{X1}R_{X2}+SC_2R_{X2}-SC_2R_{X1}+K=0$,

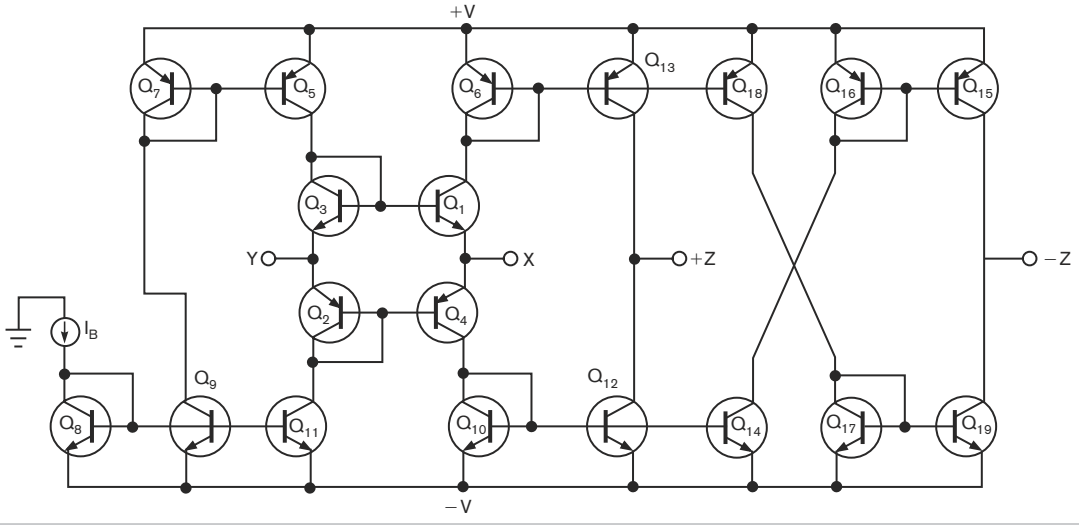

Figure 2 A current-controlled circuit uses no internal resistors or capacitors.

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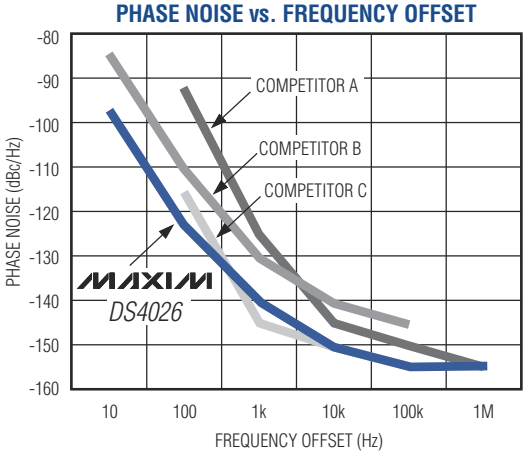
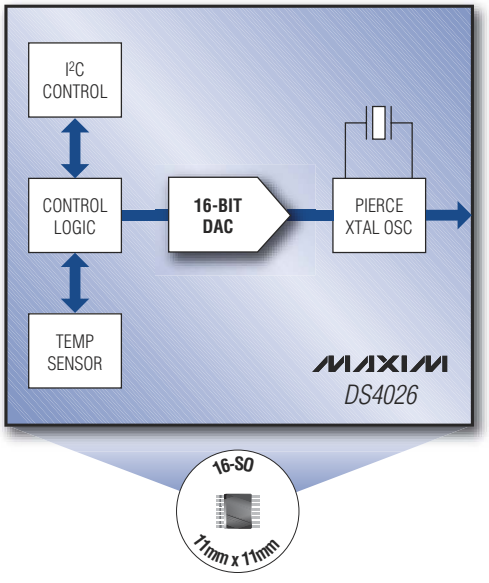
The DS4026 is an extremely accurate TCXO for wireless applications, SONET/SDH systems, instrumentation, and test systems. It is guaranteed accurate and stable to better than ±1ppm over the -40°C to +85°C industrial temperature range and better than ±4.6ppm under all conditions. With an integrated 16-bit control DAC, frequency trimming is accomplished by I²C control with resolutions better than 2ppb and ranges greater than ±8ppm. The device operates from a 3.3V ±5% supply voltage and is packaged in a standard 300-mil, 16-pin SO.





- < ±1ppm accuracy
- Overall stability of < ±4.6ppm under all conditions
- Integrated 16-bit DAC for tuning
- Integrated temperature sensor with ±3°C accuracy
- I²C control interface
- Phase noise: < -140dBc at 1kHz frequency offset
- 12.8MHz to 51.84MHz frequency range
- Custom frequencies available

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where K is the voltage multiplier. Satisfying Barkhausen's criteria—that the loop gain is unity or greater and that the feedback signal arriving back at the input is phase-shifted 360°—the required condition for oscillation is $R_{X1}=R_{X2}$, and the frequency of oscillation is $f=1/2\pi\sqrt{k/(C_1C_2R_{X1}R_{X2})}$.

Clearly, you can use the gain buffer to vary the frequency of oscillation, which is the area in which this circuit differs from the earlier Design Idea. You can use both current and voltage to control the voltage multiplier. The circuit lets you vary the voltage multiplier by adjusting bias currents I_{B3} or I_{B4} (**Figure 4**). For voltage control over K, you can use another circuit simply by using a noninverting op amp and replacing the resistors with MOSFETs working in that triode region. That approach simulates voltage-controlled resistors.

The circuit in **Figure 2** underwent testing with a PR100N PNP transistor and an NPN NP100N transistor of the bipolar arrays ALA400 and a dc supply of ±3V (**Reference 2**).

The circuit requires only two current-controlled conveyors, two grounded capacitors, and a voltage multiplier; it requires no floating capacitors and no external resistors, which makes the circuit's power consumption lower than that of RC oscillators. For a conventional bipolar-transconductance operational amplifier, the transconductance, g_m, is $I_B/2V_T$. Comparing this figure with the equivalent value of I_B, the transconductance of the bipolar-transconductance op amp is four times less than that of a dual-output current-controlled conveyor. Thus, the power consumption of the current-controlled-conveyor-based circuit is about four times less per active device than that of the op-amp-based circuit. The sensitivity study shows that $S^{\omega C}_{K;RX1;RX2;C1;C2}=-½$; ωc sensitivities are hence less than unity, which is an attractive feature of this circuit. Remember that creating an accurate oscillator model requires modeling equations to be nonlinear, and meeting the Barkhausen criteria is a necessary condition for oscillation. Oscillator circuits may latch up and never oscillate even if you satisfy the Barkhausen criteria.EDN

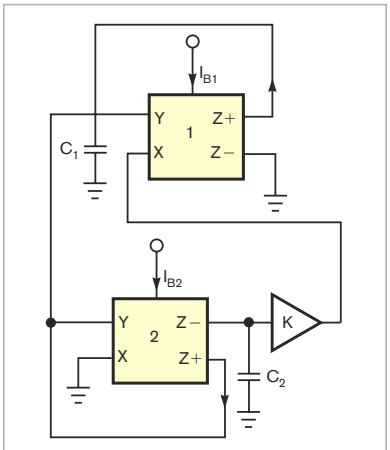

Figure 3 This configuration creates an oscillator from two current-controlled conveyor circuits.

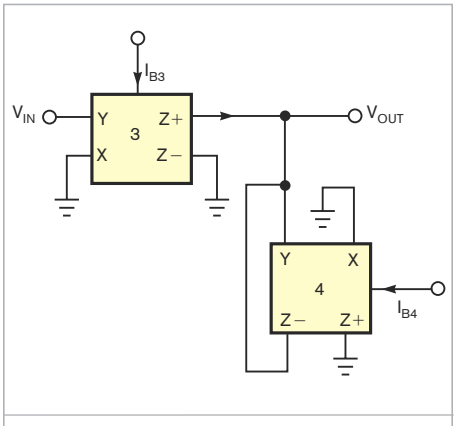

Figure 4 This circuit lets you vary the voltage multiplier by adjusting bias currents I_{B3} or I_{B4}.

REFERENCES

1 Lahiri, Abhirup, "Oscillator uses dual-output current-controlled conveyors," *EDN*, Nov 13, 2008, pg 62, www.edn.com/article/CA6611645.

2 Frey, DR, "Log-domain filtering: an approach to current-mode filtering," *Circuits, Devices and Systems, IEE Proceedings G*, 1993, Volume 140, pg 406, http://ieeexplore.ieee.org/Xplore/login.jsp?url=/iel1/2211/6397/00250002.pdf?arnumber=250002.

Perform timing for microcontrollers without using timers

Ganeshkumar Krishnamoorthy, NTERA Ltd, Dublin, Ireland

Microcontrollers now find use in every walk of life. Their peripherals vary from the general-purpose I/Os to the USB interface, making them versatile for a range of products. Timing is one key part of a typical microcontroller application. Low-cost microcontrollers have one or two built-in timers and often also have a watchdog timer. Sometimes, the design requires more timers without a significant cost increase. Software timers are not suitable for time-critical application because the controller is fully occupied. The circuit in this Design Idea uses the I/O "interrupt-on-change" feature that is common in most microcontrollers to implement a medium-precision, long-period timer with low additional cost.

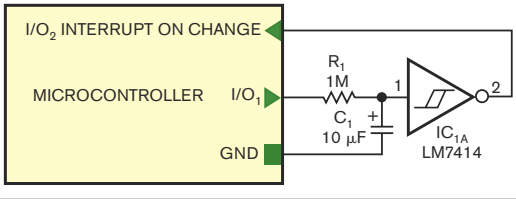

Figure 1 The RC filter along with I/O_2's interrupt-on-change feature provides a simple and cost-effective approach for a variety of time-scale measurements from microseconds to minutes.

The circuit in **Figure 1** uses I/O_1, a typical I/O pin, to drive an RC filter. The circuit feeds the output of the RC filter to a Schmitt-trigger inverter whose

output goes back to I/O_2, which has the interrupt-on-change feature. After power-up, I/O_1 is low and the output of the Schmitt-trigger inverter is high. After initialization, I/O_1 goes high. Capacitor C_1 charges up with the time constant R_1C_1. Once it reaches logic-high voltage, the output of the Schmitt-trigger inverter goes low and triggers an interrupt on I/O_2. In the ISR (interrupt-service routine), a counter increments, driving I/O_1 low. Now, C_1 discharges through R_1. The voltage reaches logic low, again triggering an interrupt. As the cycle repeats, the value in the counter indicates time=counter×R_1C_1. The Schmitt-trigger inverter serves as a debouncer.

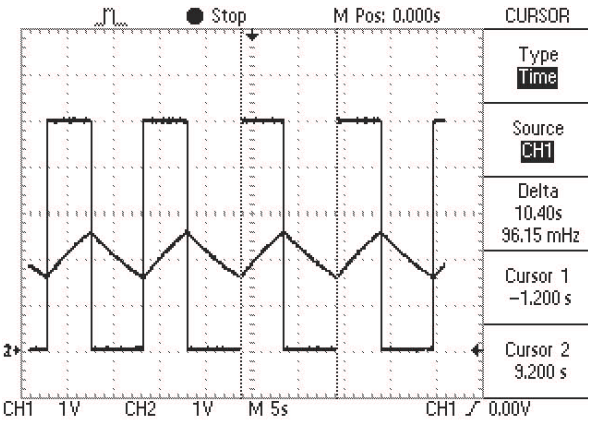

Figure 2 Channel 1 shows I/O_1's waveform, and Channel 2 shows the capacitor's charging/discharging waveform. The time period of the waveform is 10.4 sec.

Listing 1, which is available in the Web version of this Design Idea at www.edn.com/090122dia, includes the software routine for the ATMEGA64 microcontroller from Atmel (www.atmel.com). In the **listing**, Port D, Pin 5 plays the role of I/O_1 and Pin 3, whose alternate function is INT3, plays the role of I/O_2 in **Figure 1**. The trigger-edge interrupt in this case changes from falling-rising-falling edge in a cycle. Most microcontrollers don't require this feature because any logic change will trigger an interrupt. **Figure 2** shows the timing waveform of the circuit with the ATMEGA64 and the 74HC14.

The circuit's advantages are its low cost, a microcontroller-clock-independent time period, and the ability to achieve time periods of minutes to hours by tuning resistance and capacitance. For example, with a resistance of 10 MΩ, a capacitance of 10 µF, and a 16-bit register as a counter, you can achieve a maximum count of 75.85 days. EDN

ACKNOWLEDGMENT

This work is part of a system design in a project funded by the European Union under the Marie Curie Project.

productroundup

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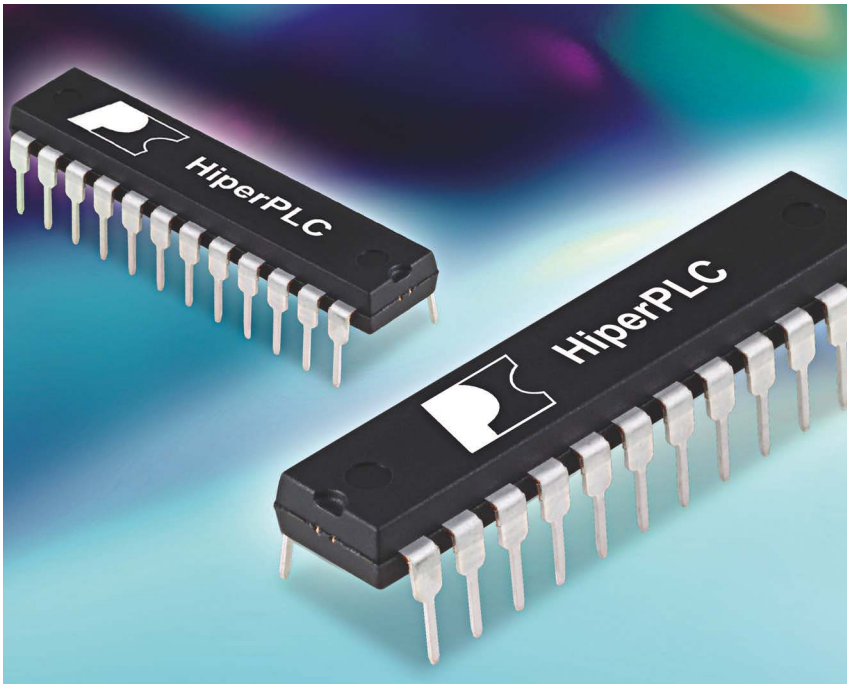


Controller IC combines resonant controller with high-voltage drivers, PFC controller

The HiperPLC high-powered, PFC (power-factor-corrected), LLC (resonant converter), power-supply-controller IC integrates a CCM (continuous-conduction-mode) PFC controller, an LLC resonant converter, and 800V half-bridge high-side/low-side driver circuitry in an IC package. The continuous-mode PFC reduces the cost of PFC magnetics by limiting ac flux, eliminating the need for Litz wire in the input choke and reducing ripple current delivered to the PFC bulk capacitor. Suiting use in flat-panel televisions and high-brightness-LED streetlights, the IC features a high-efficiency ZVS (zero-voltage-switching) LLC and off-time PFC control, eliminating ac-input-sensing components. The HiperPLC costs $2 (10,000).

Power Integrations, www.powerint.com

Autocalibration design kit interfaces with optoelectronic-sensor components

Allowing compensation for device-to-device variation in optoelectronics, the OCV100 automatic-calibration design kit calibrates reflective or interruptive devices. This feature allows designers to compensate for variations from manufacturing differences, temperature changes, power fluctuation, and device aging commonly present in optoelectronic systems. Requiring only an external power supply and the optical device for testing, the kit allows engineers to adapt and calibrate any of the vendor's sensors to any unique application. Four onboard lights indicate device calibration, inability to calibrate the device, and when the analog output reaches the logical trip point higher than the calibration point or lower than the calibration point.

The kit allows you to set the internal phototransistor-load resistance at 2.5, 9.6, or 24 kΩ. Prices for the OCV100 automatic-calibration design kit range from $31.94 to $42.59.
Optek Technology, www.optekinc.com

3W LED provides a full-color output

The AstraLED RGB suits use in a variety of kitchen appliances, communications equipment, medical devices, and automotive and sign applications requiring bright, intense light with low power consumption. The LED provides an ultrabright, full-color output in a ROHS-compliant, 3W, high-power RGB package. Features include 8-, 25-, and 20-lumen light intensities at currents of 300 (red), 350 (green), and 350 mA (blue), respectively, and a −30 to +85°C operating-temperature range. Measuring 10×16×3.3 mm, the AstraLED RGB costs $4.

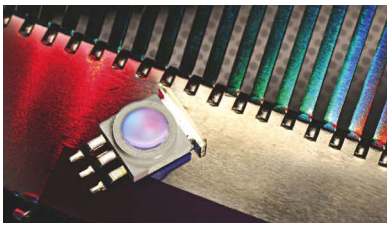
Lumex, www.lumex.com

High-brightness LED driver claims 92% efficiency

Aiming at boost, buck-boost, SEPIC (single-ended-primary-inductance-converter), and high-side buck topologies, the MAX16834 current-mode high-brightness-LED driver integrates a high-side current-sense amplifier, a PWM-dimming MOSFET driver, and robust protection circuitry. The device has 92% input-power-factor correction, requiring no additional PFC controller. This feature, along with thermal-foldback protection, suits the device for MR16 spotlights and similar applications receiving power from ac-voltage sources. Available in a thermally enhanced 4×4-mm TQFN-20 package with an exposed paddle, the MAX16834 costs $1.24.
Maxim Integrated Products, www.maxim-ic.com

650-nm fiber-optic transceiver provides termination for bare POF

The Ethernet Optolock transceiver combines a pair of fast-Ethernet fiber-optic components in a miniature housing to provide instant termination for bare POF (plastic optical fiber). Integrating a CMOS LED driver IC, the POF port improves the connection in communications and infotainment networks. The resonant-cavity LED-based 650-nm fiber-optic device has a small emission aperture and provides a fast-Ethernet communication link over POF. Compatible with both LVDS (low-voltage-differential-signaling) and CML (current-mode-logic) technologies, the device



enables designers to perform on-site cutting and termination of the fiber to the required length. Suiting 1.5- or 2.2-mm POFs, the Ethernet Optolock transceiver costs $5 (high volumes).
Firecomms, www.firecomms.com

COMPUTERS AND PERIPHERALS

Graphics card targets business applications

Using DisplayPort connectors, the Quadro NVS 450 graphics card supports as many as four digital

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displays at 2560×1600-pixel resolutions each on LCD, DLP, and plasma displays. Targeting business-graphics applications, the graphics card uses CUDA parallel-computing processors and a unified design for dynamic GPU-resource allocation. PCIe (PCI Express) 2.0 compliance provides a 5-GTbps-per-lane bidirectional transfer rate for an 8-Gbps aggregate bandwidth in each direction. The Quadro NVS 450 graphics card costs $499.

Nvidia, www.nvidia.com

Unified serial HBA family supports 128 SATA or SAS storage devices

The Series 1 unified serial HBA (host-bus-adapter) family features the 1405 and 1045 low-profile cards, supporting as many as 128 SATA or SAS storage devices. The 1405 integrates four internal ports, and the 1045 provides four external ports. The devices suit systems requiring connectivity to hard disks, tape drives, removable media, solid-state drives, RBODs (RAID bunch of disks), expanders, and JBODs (just a bunch of disks). The 1405 kit, the 1405 single, and the 1045 single cost $190, $160, and $190, respectively.

Adaptec, www.adaptec.com

COMPUTERS AND PERIPHERALS

8-Gbit Pico-C USB drive comes in 18-carat gold

The STC8GBPCKG 18-carat solid-gold USB drive supports data-transfer speeds as great as 30 Mbytes/sec. The water-resistant, 8-Gbit Pico-C drive includes FIPS-certified AES-256 encryption software. The gold STC8GBPCKG Pico-C drive costs $599.

Super Talent Technology, www.supertalent.com

LCD monitor has 96% coverage of AdobeRGB

Providing 1680×1050-pixel native resolution, the 22-in. MultiSync P series P221W LCD monitor features AmbiBright automatic brightness adjustment and internal, 10-bit, programmable look-up tables. Using XtraView+, the monitor provides a 178° (88°/88°/88°/88°) viewing angle on a four-way ergonomic stand allowing tilt, swivel, pivot, and height adjustments. Additional features include a color gamut achieving 96% coverage of AdobeRGB, a 16-msec response time, a 1000-to-1 typical contrast ratio, and a 300-cd/m^2 typical brightness. The device receives analog- and digital-input signals. The 22-in. MultiSync P Series P221W LCD monitor costs $636.90.

NEC Display, www.necdisplay.com

Memory modules target Intel's Core i7 processor

Aiming at the Intel Core i7 processor's triple-channel memory controller enables the Triple Pack Memory modules to support 1333-, 1600-, and 1866-MHz DDR3 memory speeds. The kits feature three 1- or 2-Gbyte modules, providing 3- or 6-Gbyte kits. The 1600- and 1866-MHz kits feature the vendor's Dominator memory modules, and the 1866-MHz kits include an airflow fan. Based on memory speed, prices for the six Triple Pack Memory modules range from $120 to $475.

Corsair, www.corsair.com

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BY ROY GARDNER • SUPERIOR TECHNICAL

Crystal clear

DANIEL VASCONCELLOS

Years ago, I was on a team working for All American Racers in Santa Ana, CA. During a test session, the sound of our team's newly designed Indy car screaming by at 180 mph made it difficult for us to identify the bothersome interference problems in our 460-MHz FM car-to-pit radio-communication system. We moved our equipment to a picnic table in the infield where there was less ambient noise and settled down to figure out why it was so hard for the driver and the race engineer to communicate. The racing season was coming up, and we needed a reliable radio for race-strategy communications.

The team was made up of world-class mechanical geniuses, but they were afraid of "wires." In the good old days, the only cabling on an Indy car was a single 12-gauge wire running from the magneto to the kill switch on the dashboard. Our more modern contender had miles of daunting wiring for the engine-control unit, the data-acquisition harness, telemetry, and the voice-communication system.

One of my first assignments was helping to identify and eliminate the radio interference. The mechanics could describe whatever it was as simply "noise." My supervisor felt that we should and could be a bit more specific.

Research at the shop had suggested a number of possibilities. A 50-kV ignition system is always a suspect. I tried to apply my experience with high-end stereos and remembered the way that metal body panels of luxury cars connect to each other with stout ground straps and that the front wheels have copper electrical-contact springs under the wheel-bearing caps to prevent interference. A passage in our ham-radio bible intrigued us; it spoke briefly of putting "tire powder" inside automobile tires to stop tire-generated static.

We put on our own headsets and listened to the driver and the engineer. I recognized minor amounts of electrical static, FM interference, and wind noise, but the major problem sounded to me like plain old acoustic noise from the engine's exhaust. The driver's helmet had a good noise-canceling military pilot's microphone, and he kept the mike as close as possible to his lips, but the noise level remained unacceptable.

After some brainstorming, we disconnected the driver's microphone and instructed him to press the push-to-talk button on his steering wheel while he was out doing laps. The noise remained. The radio was soft-mounted in the chassis like the rest of the electronics to prevent damage from the tremendous vibration caused by the hard-mounted engine, so we made sure the foam hadn't fallen out. We double-checked that the normally handheld radio's original microphone was still unplugged internally. Somehow, magically, the deaf radio was determined to listen to the engine's 850-horsepower holler as much as the driver's one-man-power mouth. Beating a spare radio with a hammer on our table produced similar results. Disassembling the radio and hammering the circuit board suggested a problem with the PLL (phase-locked-loop) circuitry.

More research revealed that most PLL radios are inherently microphonic—normally, to a negligible extent. It looked as though we shouldn't have placed our major-brand radio 2½ feet away from an unmuffled, 12,000-rpm, turbocharged V8 engine at full song! We had some older crystal radios still in a cabinet, and we tried one at the next test expedition before modifying a PLL unit. Voilà! My supervisor felt we had ourselves a "speed secret" and instructed us not to tell any other team. But we're still wondering what the story is on the mysterious tire powder. EDN

Roy Gardner has tamed electrons for several major electronics firms and Indy car teams.

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